COMPARISON OF CNTFET AND MOSFET NOISE PERFORMANCE THROUGH THE DESIGN OF BASIC CURRENT MIRROR

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ABSTRACT

In this paper we present a comparative analysis of noise performance of Carbon Nanotube Field Effect Transistors (CNTFETs) and MOSFET, through the design of a basic current mirror.

We show the output I-V curves, the output differential conductances at various output voltages, the output admittance at various frequencies and the spectral density of output noise current.

For reference current of 1 μA and 10 μA the output static and dynamic characteristics are better in the case of CNTFET, but for all cases the output noise current is always higher for the CNTFET than for the MOS.

The software used is Advanced Design System (ADS) which is compatible with the Verilog A programming language.

Keywords: *CNTFET, MOSFET, Modelling, Current Mirror Design, Advanced Design System (ADS).*

1. INTRODUCTION

MOSFET technology has continued to scale to ever-smaller dimensions. However, at smaller dimension various problems like mobility degradation, source to drain tunneling, random dopant fluctuations, device mismatch etc. crop up, that affect device performance and reliability inhibiting further scaling.

A promising candidate which avoids these difficulties and allows further scaling down is the Carbon Nanotube Field Effect Transistor (CNTFET). CNTFET is a new kind of molecular device, using a carbon nanotube as channel [1-7]. Among carbon nanotube FETs, conventional CNTFET (also denoted as C-CNTFET), with heavily doped source and drain contacts, is utilized for high-performance and low-power memory designs, also because this device has a significantly smaller off current which greatly reduces the power consumed at off state of CNTFET [8-9].

For this device we have already proposed a compact, semi-empirical model [2-8], in which we introduced some improvements to allow an easy implementation both in SPICE and in Verilog-A. Then our model has been implemented to carry out static and dynamic analysis of A/D circuits [10-15].

In this paper we present a comparative analysis of noise behavior of CNTFETs and MOSFET devices through the design of a basic current nirror. To have comparable results, we refer to a C-CNTFET and a MOSFET in 32 nm technology.

The software used is Advanced Design System (ADS) which is compatible with the Verilog A programming language. The simulation results allow to show the differences between CNTFET and MOS technology and the advantages of the first for analogue VLSI circuits.

The presentation of the paper is organized as follows. At first we present a brief review of the CNTFET and MOSFET models used in the proposed designs. Then we show and discuss the simulation results together with conclusions and future developments.

2. A BRIEF REVIEW OF CNTFET AND MOSFET MODEL USED

An exhaustive description of our I-V CNTFET model is in [14-18]. Therefore we suggest the reader to consult these References.

It is a compact, semi-empirical model directly and easily implementable in simulation software to design analog and digital circuits: in fact the most complex part of the model is contained in Verilog A [19].

With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the total drain current can be expressed as [3]:

$$I_{DS} = \frac{4qkT}{h} \sum_{p} \left[\ln\left(1+\exp\xi_{Sp}\right) - \ln\left(1+\exp\xi_{Dp}\right) \right] \qquad (1)$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp}, depending on temperature through the sub-bands energy gap, and V_{CNT}, have the expressions reported in [7-9].

Regards to C-V model, an exhaustive description of our C-V model is widely described in [9] and therefore the reader is requested to consult it, in which the following expressions of quantum capacitances C_{GD} and C_{GS} are explained:

$$\begin{cases} C_{GD} = q\sum_{p} \frac{\partial n_{Dp}}{\partial V_{GS}} = q\sum_{p} \frac{\partial n_{Dp}}{\partial \xi_{Dp}} \frac{\partial \xi_{Dp}}{\partial V_{CNT}} \frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS} = q\sum_{p} \frac{\partial n_{Sp}}{\partial V_{GS}} = q\sum_{p} \frac{\partial n_{Sp}}{\partial \xi_{Sp}} \frac{\partial \xi_{Sp}}{\partial V_{CNT}} \frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad (2)$$

In order to simulate correctly the CNTFET behaviour, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances.

In this paper we have achieved this goal using an empirical method [2-3] more suitable for simulations in CAD environment. This method requires the extraction of the previous parasitic elements comparing the device characteristics with the measured ones. In this way all elements of the equivalent circuit can be determined [2-3].

Fig. 1 shows our model, in which we have reported the values of circuital elements, while Fig. 2 shows its symbol, that we will use in the following simulations.

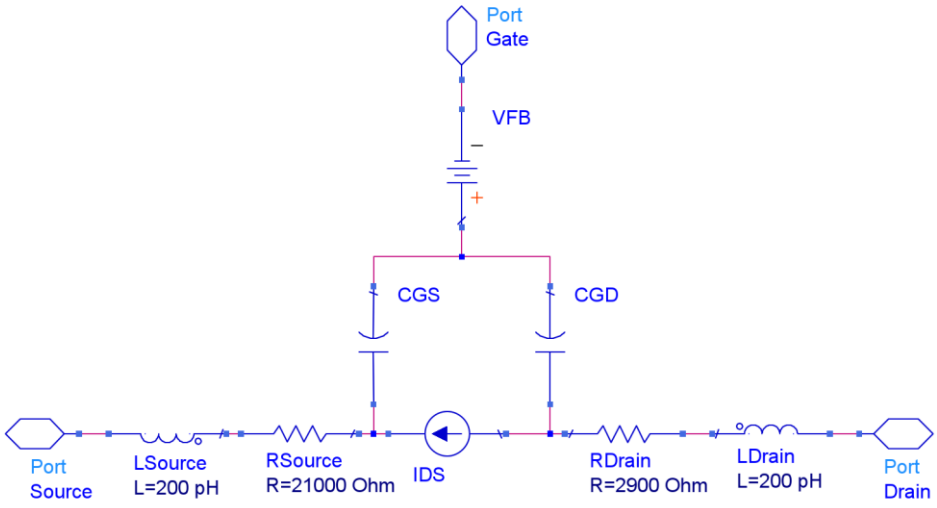

Figure 1. Equivalent circuit of n-type CNTFET.

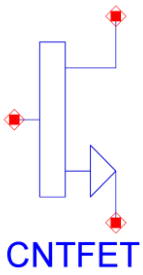

Figure 2. Symbol of our model.

For the MOSFET model we use the **BSIM4 model** of ADS library.

BSIM (Berkeley Short-channel IGFET Model) [20] refers to a family of MOSFETs for integrated circuit design. It also refers to the BSIM group located in the Department of Electrical Engineering and Computer Sciences (EECS)

at the University of California, Berkeley, that develops these models. In this work BSIM4 has been used for the 32 nm technology nodes.
Moreover the MOSFET parameters, obtained using an evolution of previous Berkeley Predictive Technology Model (BPTM), are improved by us through parametric simulations to obtain performance of the MOSFET model comparable to the CNTFET one.
Fig. 3 shows the MOSFET symbol, which refers to BSIM4 model.

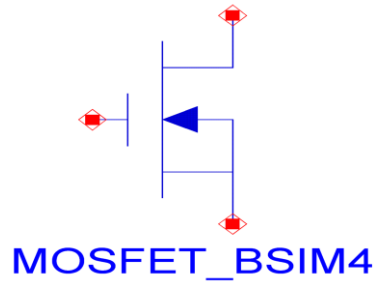

Figure 3. MOSFET symbol.

Regards to noise model, in [21] we have proposed a compact noise model of CNTFET, and therefore we suggest the reader to consult this paper.
Fig. 4 shows the proposed CNTFET noise model, including five different noise sources.

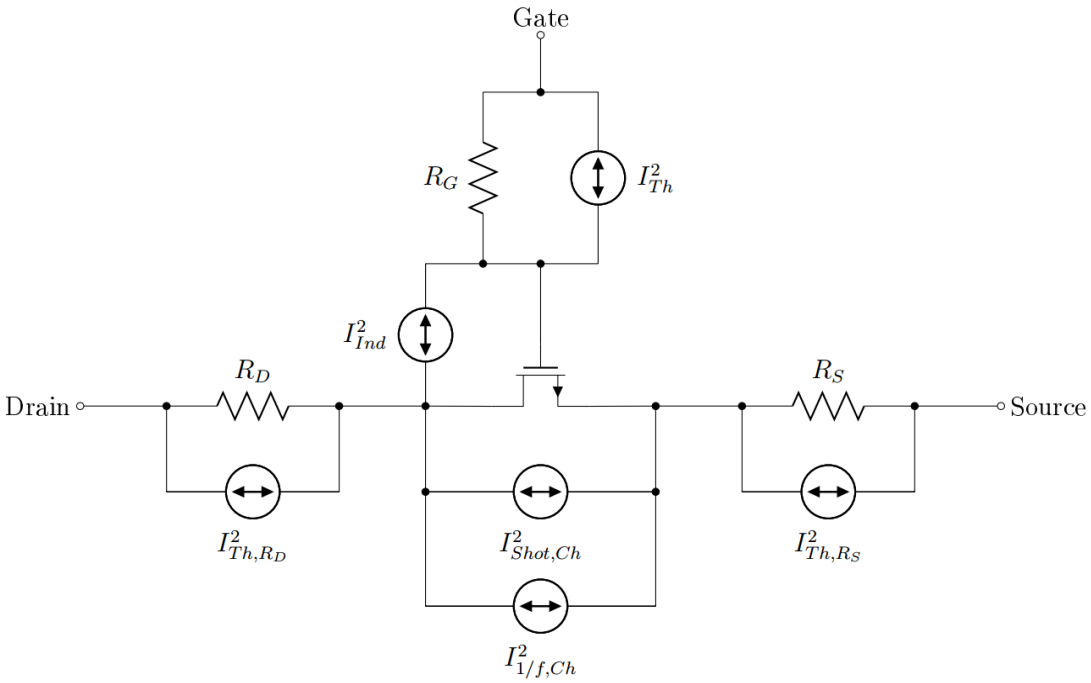

Figure 4. The proposed CNTFET noise model, including the main noise sources [21].

In particular we have considered the main noise sources, which are [21]:

1. Thermal noise of R_G
2. Thermal noise of R_S and R_D
3. Channel thermal noise and shot noise
4. Flicker noise
5. Channel-induced gate noise.

For an exhaustive analytical description of our CNTFET noise model we suggest the reader to consult our Reference [21].

3. BASIC CURRENT MIRROR

The basic current mirror is the keystone of the current mirror circuits and it consists in just two active component as shown in Fig. 5.

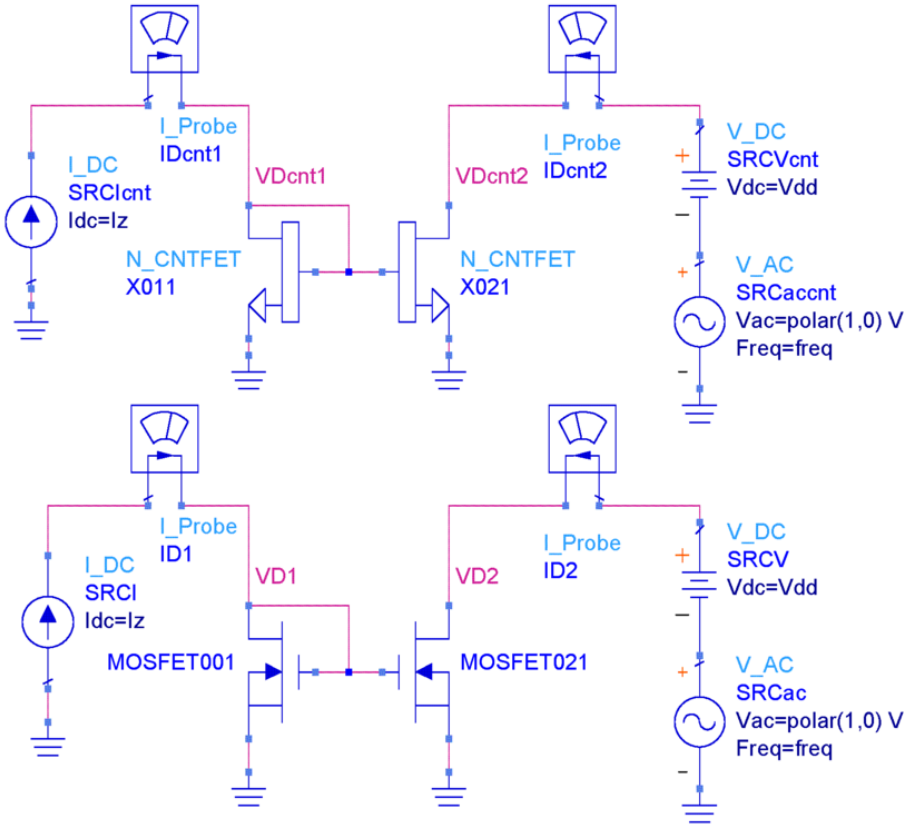

Figure 5. Basic current mirror: on top the CNTFET version, on bottom the MOS version.

In this circuit the reference current is injected by the current generator on the far left side, the two active devices mirror this current on the output, on the right side. The constant voltage generator is plug in series to the output to force the output voltage. The AC voltage generator is used to obtain the output resistance at various frequencies.

We ran fist a static simulation to measure the output behavior of the circuit when the output if forced at various voltages. We first plot ratio of the output current to the input current, since in a current mirror it should be 1.

In Fig. 6 we present the obtained results for CNTFET and MOS circuit having considered three input currents, 1 uA (in red), 10 uA (in blue) and 100 uA (in violet). This scheme will be repeated in all following analysis and therefore we will no more stress this.

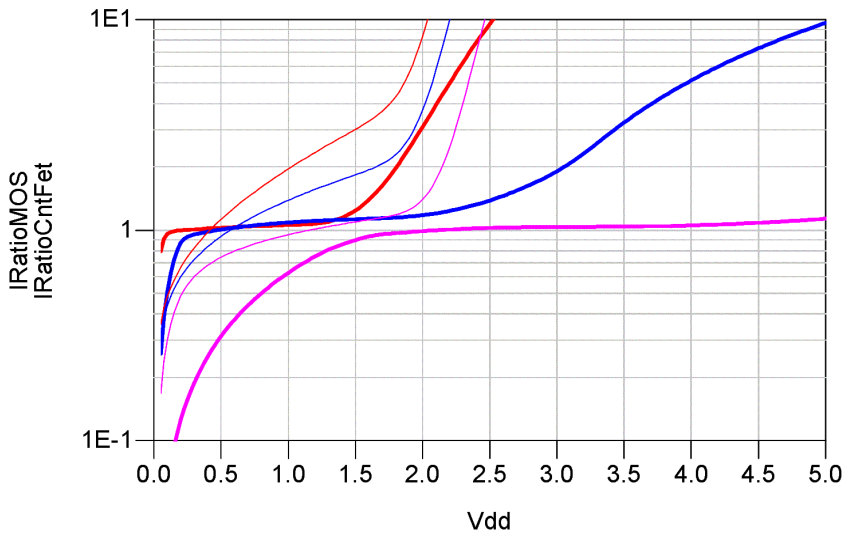

Figure 6. Ratio of the output current divided to the input current. For the CNTFET circuit the curves are bold lines, while for the MOS circuit the curves are thin lines.

We note that for the CNTFET the ratio is near to 1 for a larger interval of output voltage values, indeed for the MOS circuit the ratio is not stable near the value of 1.

In the CNTFET case the 1 uA current the ratio is stable from 0.1 V to 1.5 V, the 10 uA has a good output voltage interval between 0.3 V and 2.5 V, while the 100 uA current has a ratio near 1 at voltages greater than 1.5 V.

Fig. 7 shows the differential output resistance of the circuit, defined as the derivative of the I-V output static curves.

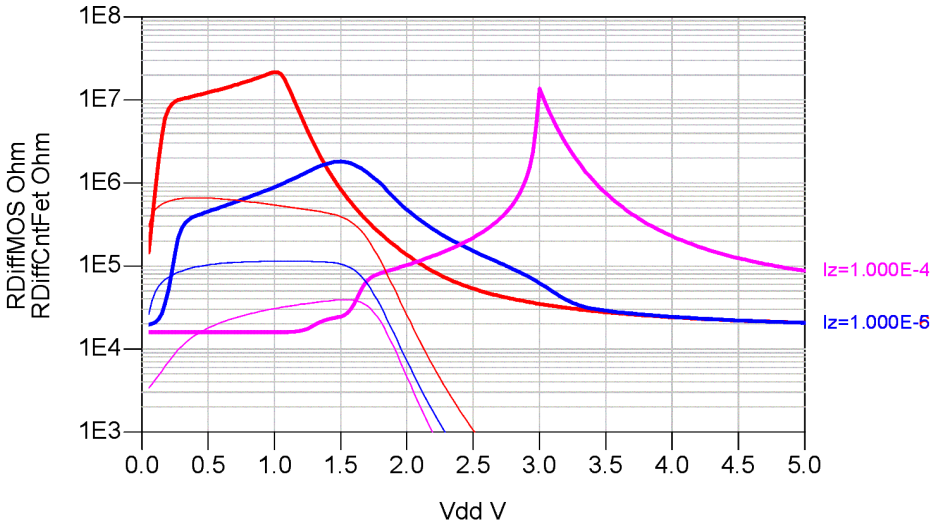

Figure 7. Differential output resistance of the current mirror circuits. Lines as in Fig. 6.

Here we observe that the higher resistance values are in the same intervals where the current ratio is near 1, as expected. Moreover we observe that the CNTFET circuit has almost always an higher output resistance than the MOS circuit.

In the second simulation we studied the frequency behaviour of the output admittance for small signal in linearized approximation and the obtained results are shown in Figs. 8 and 9. The output voltage is held constant at 1 V for all the currents.

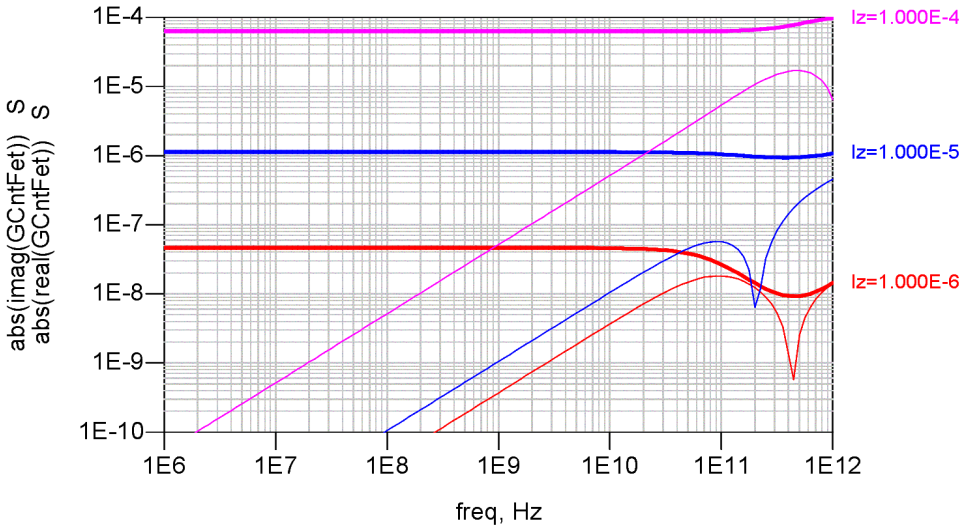

Figure 8. Differential output admittance for the CNTFET circuit, values in Siemens. The real part is in bold lines, the imaginary part in thin lines.

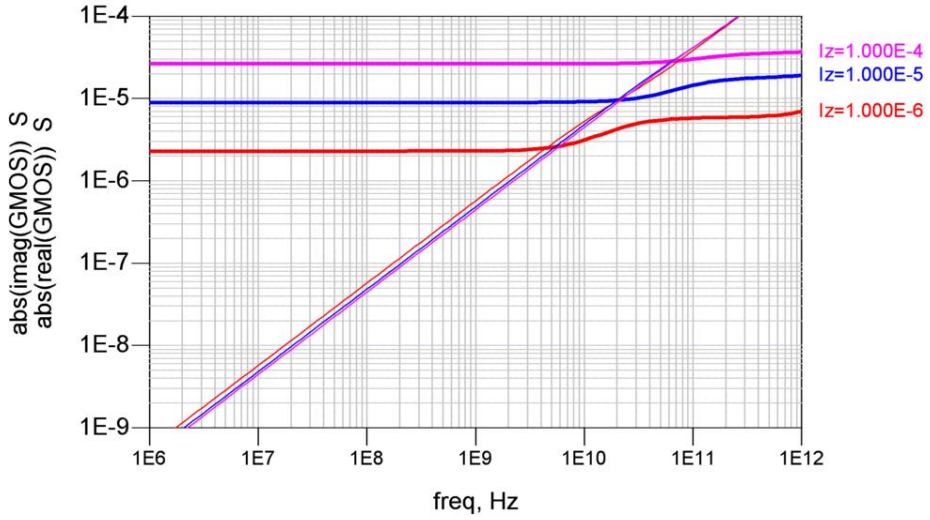

Figure 9. Differential output admittance for the MOS circuit, values in Siemens. The real part is in bold lines, the imaginary part in thin lines.

We can observe that while the real part is almost independent from the frequency, the imaginary part (at frequency lower than 100 GHz) is just proportional to the frequency, so that, at lower frequency, the differential output circuit could be represented as a parallel of a resistor, a capacitor and the current generator.
As third analysis we present the noise simulations at output voltage 1 V.
Fig. 10 shows the spectral density of the output noise current for both CNTFET and MOS at different currents.

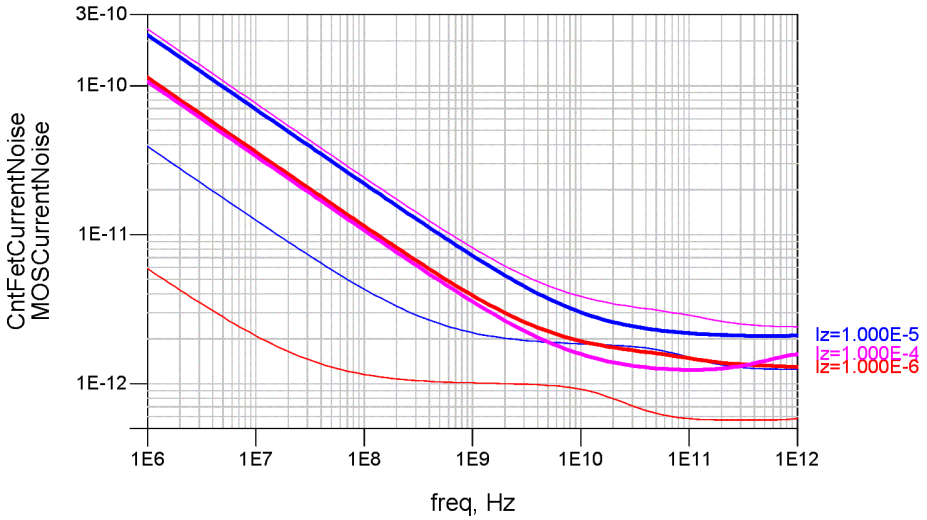

Figure 10. Spectral density of the output noise current for the CNTFET and for the MOS circuit, values in A Hz$^{-1/2}$. Lines as in Fig. 6.

We can see higher noise in the CNTFET circuit in almost all cases, but over 1 GHz it is no more than three times higher, as shown in Fig. 11.
In the case of 100 uA current, the noise in lower for the CNTFET circuit.

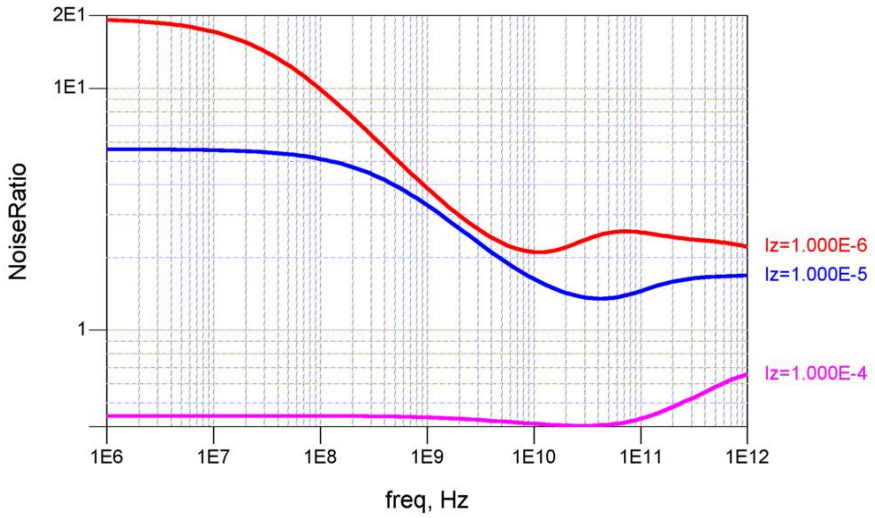

Figure 11. Ratio of the noise current spectral density of the CNTFET circuit divided by the noise current spectral density of the MOS circuit.

We also calculate the spectral density of noise current for the component coming from the flicker, the shot and the thermal noise coming from input and output devices for the CNTFET circuit.
Except the case of the 100 μA current, devices contribute evenly to the output noise in the lower frequency range. Since the main idea of the current mirror is just mirroring current, it was easy to understand how the noise current on the input branch is mirrored in the output branch when the circuit is properly working.

In the CNTFET, compared to BSIM4 MOS model, for frequencies below 10 GHz the main contribution is the flicker noise which largely dominates for its 1/f dependence. For frequency over 10 GHz the main contributor are the shot noise and the thermal noise.
Since the thermal noises is proportional to the resistances, its reduction requests a better control of the various parasitic resistances, always considering that the limit for channel resistance is the quantum limit.
We also observe that the effect of correlation between channel current noise and the current noise induced in the gate, has a negligible effect on the overall result, as predicted in [22].

4. CONCLUSION AND FUTURE DEVELOPMENTS

We have presented a simulation study of a based current mirror based on CNTFET, comparing it with the same using MOS device and showing the output I-V curves, the output differential conductances at various output voltages, the output admittance at various frequencies and the spectral density of output noise current.
For reference current of 1 μA and 10 μA the output static and dynamic characteristics are better in the case of CNTFET, but for all cases the output noise current is always higher for the CNTFET than for the MOS.
The output noise for CNTFET is no more than three times higher (10 dB) than for the MOS, but at some frequency and current we foresee no more than two (6 dB) times higher.
In order to make further comparisons, we are considering other circuits, using also other CNTFET models [23-24].
Currently we are working to study the effect of temperature [25-28].and of noise in the CNTFET-based design of analog and digital circuits.

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