ANALYSIS OF CNTFET AND MOSFET PERFORMANCE THROUGH THE DESIGN OF AMPLIFIERS IN SOURCE AND DRAIN COMMON CONFIGURATION

Roberto Marani[1] and Anna Gina Perri[2]
[1] National Research Council of Italy (CNR), Institute of Intelligent Industrial Technologies and Systems for Advanced Manufacturing (STIIMA), Bari, 70125, Italy
[2] Department of Electrical and Information Engineering, Polytechnic University of Bari, 70125, Italy
E-mail: annagina.perri@poliba.it

ABSTRACT
We present a comparative analysis of Carbon Nanotube Field Effect Transistors (CNTFETs) and MOSFET devices, through the design of an amplifier both in source and drain common configuration. In particular the CNTFET used is a C-CNTFET and the MOSFET is in 32 nm technology, in order to have comparable results.
We show how the use of CNTFETs improves the performance of proposed circuits with regards to the pass band, gain and output resistance. All simulation results are performed in Verilog-A, avoiding so the problems presented in SPICE used in previous designs, proposed in literature.

Keywords: *CNTFET, MOSFET, Modelling, Amplifier Design, Advanced Design System (ADS).*

1. INTRODUCTION

Carbon NanoTube Field Effect Transistors (CNTFETs) are a new kind of molecular device, using a carbon nanotube as channel, and are able to work better at nanometer scale, which is the ultimate limit in miniaturization [1-7].
In particular conventional CNTFETs (C-CNTFETs) are utilized for high-performance and low-power memory designs, also because this device has a significantly smaller off current which greatly reduces the power consumed at off state of CNTFET [8-9].
For this device we have already proposed a compact, semi-empirical model [2-8], in which we introduced some improvements to allow an easy implementation both in SPICE and in Verilog-A. Then our model has been implemented to carry out static and dynamic analysis of analogue and digital circuits [10-15].
In this review we present a comparative analysis of CNTFETs and MOSFET devices through the design of an amplifier in source and drain common configuration. In order to have comparable results, we refer to a C-CNTFET and a MOSFET in 32 nm technology.
The software used is Advanced Design System (ADS) which is compatible with the Verilog A programming language. The simulation results allow to show the differences between CNTFET and MOS technology and the advantages of the first for analogue VLSI circuits.
The presentation of the paper is organized as follows. After a brief review of the CNTFET and MOSFET models used, we show and discuss the simulation results together with conclusions and future developments.

2. A REVIEW OF CNTFET AND MOSFET MODEL USED

An exhaustive description of our CNTFET model is in [14-18]. Therefore we suggest the reader to consult these References. It is a compact, semi-empirical model directly and easily implementable in simulation software to design analog and digital circuits: in fact the most complex part of the model is contained in Verilog A [19].
In particular, the software used is Advanced Design System (ADS) which is compatible with the Verilog A programming language. We have considered a single wall n-CNTFET in the ballistic transport hypothesis. This assumption allowed to define an analytical formula for CNT current.
When a positive voltage V_{GS} is applied between gate-source, the conduction band at the channel beginning decreases by qV_{CNT}, where q is the electron charge and V_{CNT} is the surface potential, whose expression is reported in our References [13-16].
With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the total drain current can be expressed as [3]:

$$I_{DS}=\frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \quad (1)$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp}, depending on temperature through the sub-bands energy gap, and V_{CNT}, have the expressions reported in [3].
In order to simulate correctly the CNTFET behaviour, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances. In this paper we have achieved this goal using an empirical method (2-3), more suitable for simulations in CAD environment. This method requires the extraction of the previous parasitic elements comparing the device characteristics with the measured ones. In this way all elements of the equivalent circuit can be determined [2-3].
Fig. 1 shows our model, in which we have reported the values of circuital elements, used in the following simulations.

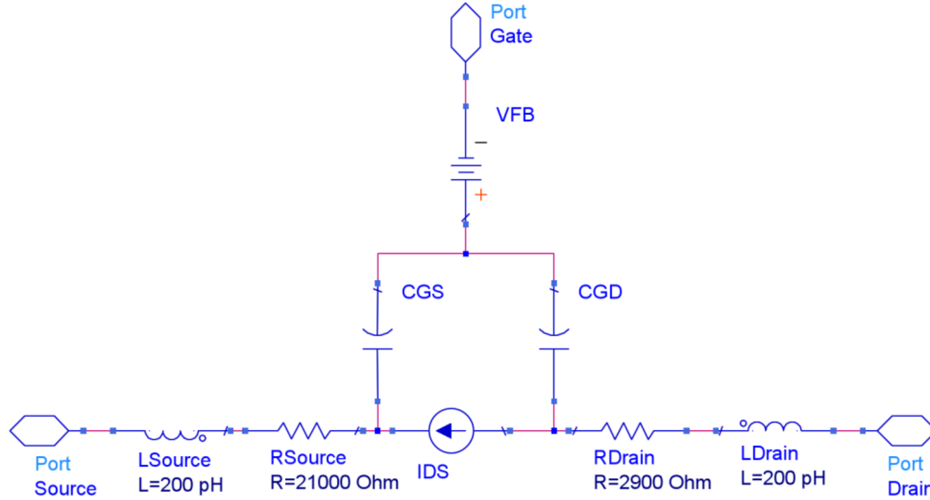

Figure 1. Our CNTFET model (named as LabDis. model).

It is similar to a common MOSFET one and is characterized by the flat band generator V_{FB}, the quantum capacitances C_{GS} and C_{GD} , the inductances of the CNT L_D and L_S and the resistors R_D and R_S, in which the parasitic effect due to the electrodes are also included.
For the MOSFET model we use the **BSIM4 model** of ADS library.
BSIM (Berkeley Short-channel IGFET Model) [20] refers to a family of MOSFETs for integrated circuit design. It also refers to the BSIM group located in the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley, that develops these models. In this work BSIM4 has been used for the 32 nm technology nodes.
Moreover the MOSFET parameters, obtained using an evolution of previous Berkeley Predictive Technology Model (BPTM), are improved by us through parametric simulations to obtain performance of the MOSFET model comparable to the CNTFET one.

3. DESIGN OF A COMMON SOURCE AMPLIFIER

In this section we compare the performances of a common source (C-S) amplifier realized both with a MOSFET and then with a CNTFET.
The circuital configurations are shown in Fig. 2 and Fig. 3 respectively.
In particular we compare the values obtained from the simulations with those obtained by theoretical calculation using the following formulas [21]:

$$A_V = -g_m\left(\frac{r_o R_D}{r_o + R_D}\right) \quad \text{and} \quad R_{OUT} = \frac{r_o R_D}{r_o + R_D} \qquad (2)$$

As the gate is isolated, the input resistance of the stage is infinite ($R_{IN} \to \infty$). Moreover $R_D = R_{LOAD}$.

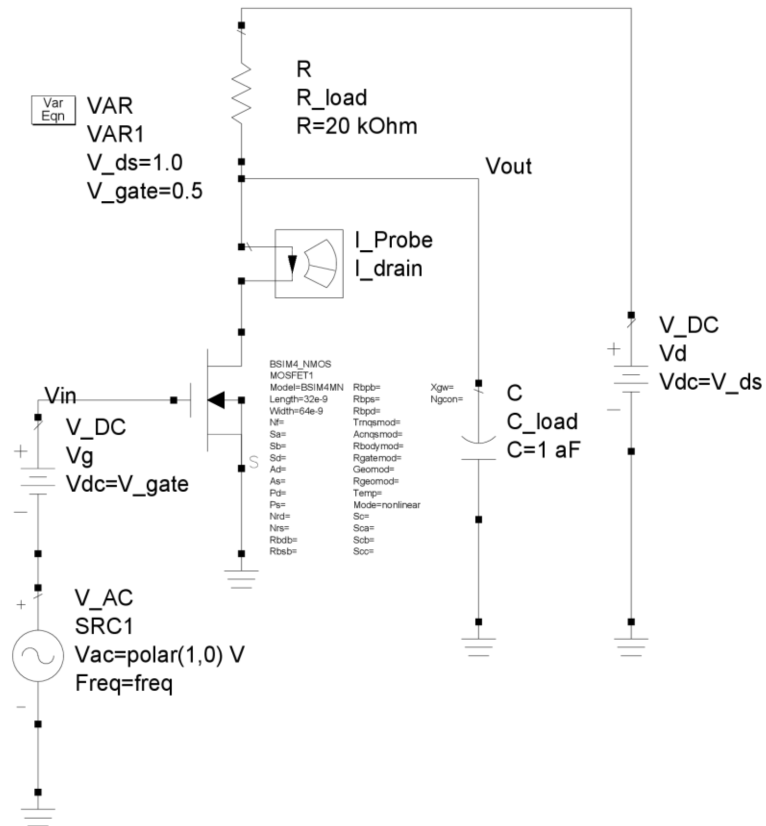

Figure 2. C-S amplifier with MOSFET in 32 nm technology.

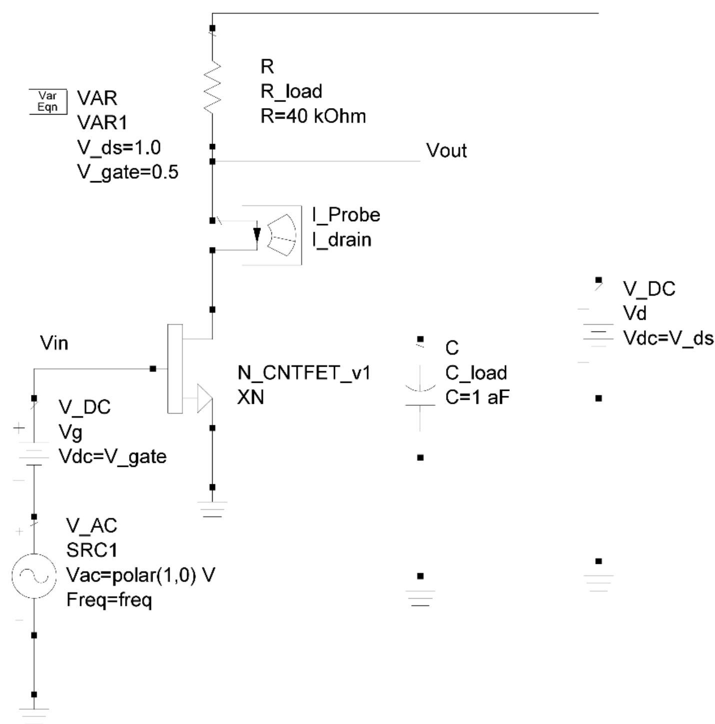

Figure 3. C-S amplifier based on CNTFET.

The analysis of the previous circuits of Figures 2 and 3 have been obtained used the parameters reported in Table 1.

TABLE 1. Parameter values.

Device	V_G	V_D	I_D	g_m	r_o
MOSFET 32nm	0.5 V	1V	16.3 μA	0.178 mA/V	9.6 kΩ
CNTFET	0.5 V	1V	6.8 μA	0.035 mA/V	200 kΩ

The simulation results are shown in Fig. 4 and Fig. 5.

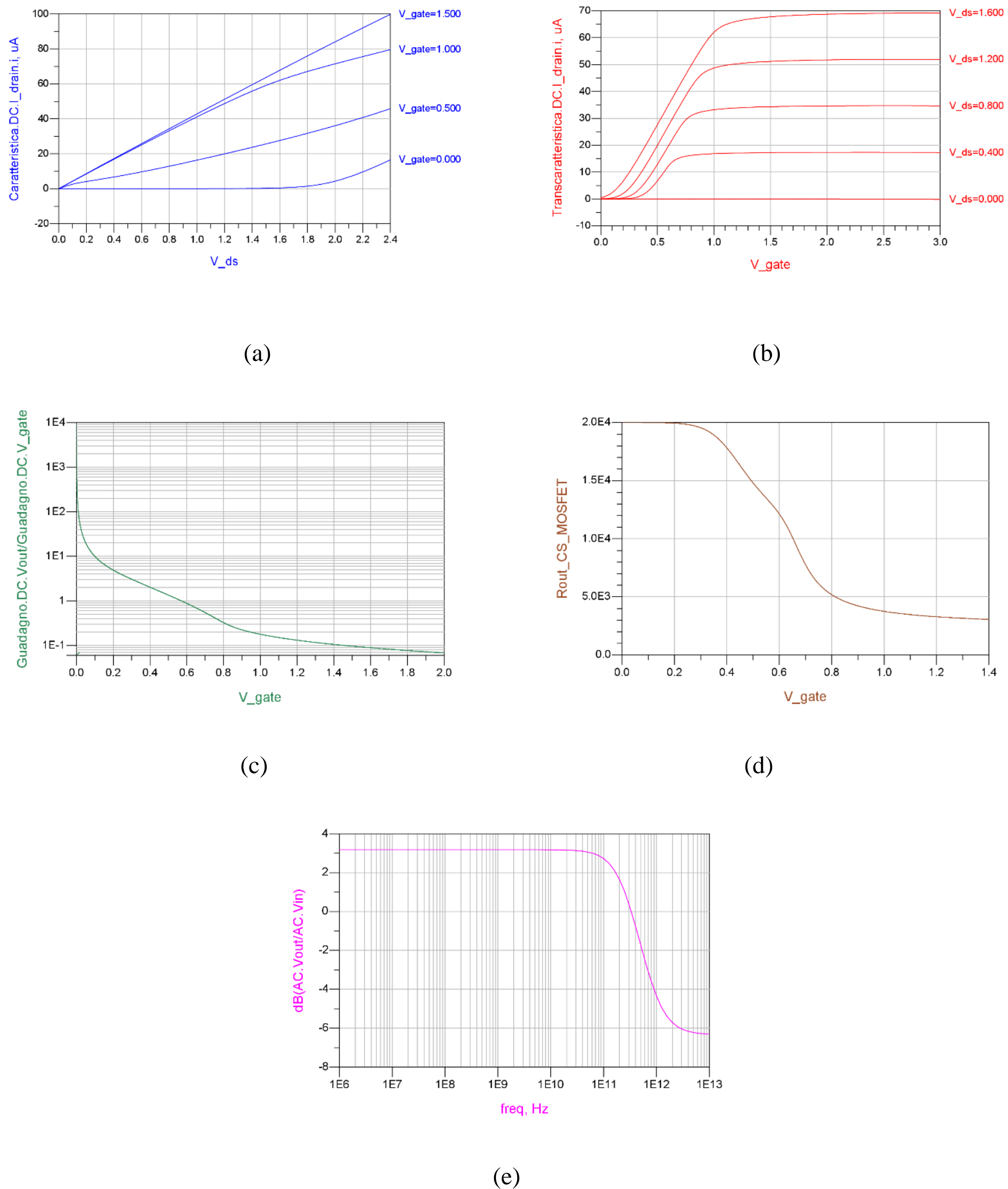

Figure 4. Simulation results for the C-S amplifier with 32 nm MOSFET: (a) output characteristics; (b) trans-characteristics; (c) voltage gain; (d) output resistance; (e) frequency response.

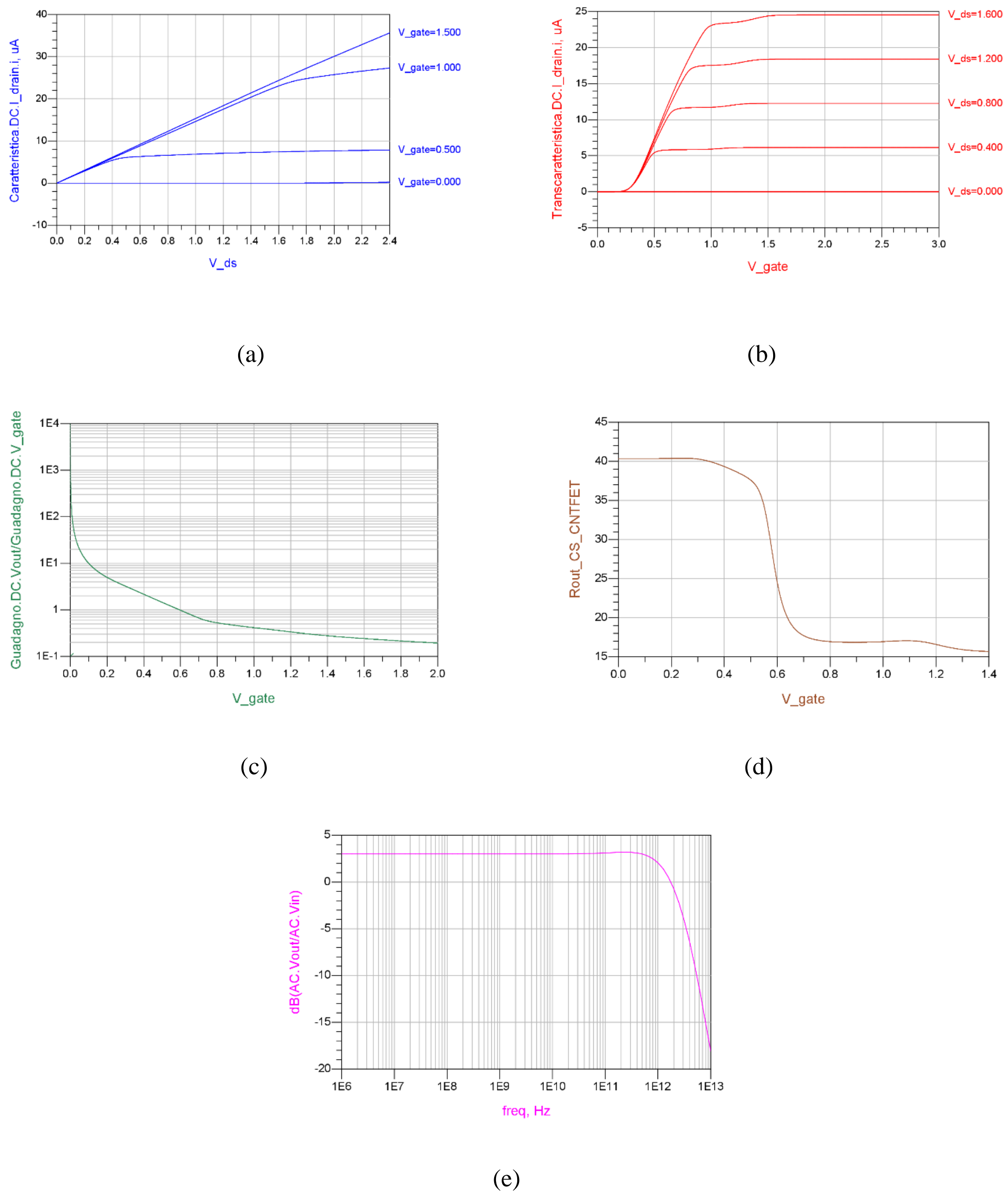

Figure 5. Simulation results for the C-S amplifier with CNTFET: (a) output characteristics; (b) trans-characteristics; (c) voltage gain; (d) output resistance; (e) frequency response.

In Table 2 we compare the values obtained from the simulations with those obtained by theoretical calculations [21].

TABLE 2. Theoretical and simulated values of A_V and R_{OUT}.

	MOSFET 32 nm		CNTFET	
	THEORETICAL VALUES	SIMULATED VALUES	THEORETICAL VALUES	SIMULATED VALUES
A_V	- 1.15	- 1.48	- 1.16	- 1.41
R_{OUT}	6.48 kΩ	14.35 kΩ	33.34 kΩ	37.45 kΩ

It is clear from the previous analysis that the use of a CNTFET rather than a MOSFET improves the performance of a common source amplifier. In fact, for equal gains, there is a halving of the current and a widening of the pass band of about 1.2 THz, being the MOSFET cut-off frequency $f_c = 316$ GHz and the CNTFET cut-off frequency $f_c = 1.5$ THz.

4. DESIGN OF A COMMON DRAIN AMPLIFIER

In this section we compare the performances of a common drain (C-D) amplifier realized both with a MOSFET and then with a CNTFET.

In particular we compared the values obtained from the simulations with those obtained by theoretical calculation using the following formulas [21]:

$$A_V = \frac{g_m (r_o // R_S)}{1 + g_m (r_o // R_S)} \quad \text{and} \quad R_{OUT} = r_o // R_S // \left(\frac{1}{g_m}\right) \qquad (3)$$

Also in this case, as the gate is isolated, the input resistance of the stage is infinite ($R_{IN} \to \infty$). Moreover $R_S = R_{LOAD}$.

The analysis have been obtained used the parameters reported in Table 3.

TABLE 3. Parameter values.

Device	V_G	V_D	I_D	g_m	r_o
MOSFET 32nm	1.5 V	3V	1.45 µA	0.053 mA/V	9.6 kΩ
CNTFET	1.5 V	3V	1.18 µA	0.035 mA/V	200 kΩ

The design technique is the same previously examined for a CS amplifier and therefore, in order to avoid overloading the discussion, we limit ourselves to report in Table 4 the values obtained from the simulations with those obtained by theoretical calculations [21].

TABLE 4. Theoretical and simulated values of A_V and R_{OUT}.

	MOSFET 32 nm		CNTFET	
	THEORETICAL VALUES	SIMULATED VALUES	THEORETICAL VALUES	SIMULATED VALUES
A_V	0.34	0.66	0.85	0.79
R_{OUT}	6.2 kΩ	1.7 kΩ	24 kΩ	21.6 kΩ

It is useful to point out that in the theoretical calculations made for the MOSFET configuration, it was possible to neglect the source resistance ($R_S = 1000$ KΩ) in parallel with the MOSFET output resistance ($r_o = 9.6$ KΩ) being R_S much greater than r_o. Moreover, also for a C-D amplifier we have a pass band of 525 GHz for MOSFET configuration and 14.4 THz for CNTFET configuration.

5. CONCLUSIONS AND FUTURE DEVELOPMENTS

WIn this paper we shown, through a comparative study of some analogue circuit based on CNTFET and 32-nm MOSFET, how it is possible to improve the performance of considered circuits.

In particular, in a common source amplifier design, for equal gains, we found a halving of the current and a widening of the pass band of about 1.2 THz, being the MOSFET cut-off frequency $f_c = 316$ GHz and the CNTFET cut-off frequency $f_c = 1.5$ THz. Same improvements have been obtained also in the common drain amplifier design.

In order to make further comparisons, we are considering other circuits, both analog and digital, using also other CNTFET models [22-23].

Currently we are working to study the effect of temperature [24-27].and of noise [28].in the CNTFET-based design of analog and digital circuits.

6. REFERENCES

[1] A. G. Perri: *Dispositivi Elettronici Avanzati*, Progedit Editor, Bari, Italy; ISBN: 978-88-6194-081-9, (2018).

[2] A.G. Perri and R. Marani, *CNTFET Electronics: Design Principles*, Progedit Editor, Bari, Italy, ISBN: 978-88-6194-307-0, (2017).

[3] G. Gelao, R. Marani, R. Diana, A.G. Perri: A Semi-Empirical SPICE Model for n-type Conventional CNTFETs, *IEEE Transactions on Nanotechnology*, **10**(3), 506-512, (2011).

[4] R. Marani, A.G. Perri: A Compact, Semi-empirical Model of Carbon Nanotube Field Effect Transistors oriented to Simulation Software, *Current Nanoscience*, **7**(2), 245-253, (2011).

[5] R. Marani, A.G. Perri: Simulation of CNTFET Digital Circuits: a Verilog-A Implementation, *International Journal of Research and Reviews in Applied Sciences*, **11**(1), 74-81, (2012).

[6] R. Marani, A.G. Perri: Modelling and Implementation of Subthreshold Currents in Schottky Barrier CNTFETs for Digital Applications, *International Journal of Research and Reviews in Applied Sciences*, **11**(3), 377-385, (2012).

[7] R. Marani, A.G. Perri: A DC Model of Carbon Nanotube Field Effect Transistor for CAD Applications. *International Journal of Electronics*, **99**(3), 427 – 444, (2012).

[8] R. Marani, G. Gelao, A.G. Perri: Comparison of ABM SPICE library with Verilog-A for Compact CNTFET model implementation, *Current Nanoscience*, **8**(4), 556-565, (2012).

[9] R. Marani, G. Gelao and A.G. Perri: Modelling of Carbon Nanotube Field Effect Transistors oriented to SPICE software for A/D circuit design, *Microelectronics Journal*, **44**(1), 33-39, (2013).

[10] R. Marani and A.G. Perri: Analysis of CNTFETs Operating in SubThreshold Region for Low Power Digital Applications, *ECS Journal of Solid State Science and Technology*, 5(2), M1-M4, (2016).

[11] R. Marani and A.G. Perri: A De-Embedding Procedure to Determine the Equivalent Circuit Parameters of RF CNTFETs, *ECS Journal of Solid State Science and Technology*, **5**(5), M31-M34, (2016).

[12] G. Gelao, R. Marani, L. Pizzulli and A.G. Perri: A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part I: Static Analysis, *Current Nanoscience*, **11**(4), 515-526, (2015).

[13] G. Gelao, R. Marani, L. Pizzulli and A.G. Perri: A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part I: Dynamic Analysis, *Current Nanoscience*, **11**(6), p. 770-783, (2015).

[14] R. Marani and A.G. Perri: A Simulation Study of Analogue and Logic Circuits with CNTFETs, *ECS Journal of Solid State Science and Technology*, **5**(6), M38-M43, (2016).

[15] R. Marani and A.G. Perri: A Comparison of CNTFET Models through the Design of a SRAM Cell, *ECS Journal of Solid State Science and Technology*, **5**(10), M118-M1, (2016).

[16] R. Marani and A.G. Perri: CNTFET-based Design of Current Mirror in Comparison with MOS Technology, *ECS Journal of Solid State Science and Technology*, **6**(5), M60-M68, (2017).

[17] R. Marani and A.G. Perri: Design and Simulation Study of Full Adder Circuit based on CNTFET and CMOS technology by ADS, *ECS Journal of Solid State Science and Technology*, **7**(6), M108-M122, (2018).

[18] R. Marani, and A.G. Perri: A Review on the Study of Temperature Effects in the Design of A/D Circuits based on CNTFET, *Current Nanoscience*, **15**(5), p. 471-480, (2019).

[19] Verilog-AMS language reference manual, Version 2.2, (2014).

[20] http://bsim.berkeley.edu/models/bsim4/

[21] A. G. Perri, *Fondamenti di Elettronica*, Editor Progedit, Bari, Italy ISBN 978-88-6194-045-1, (2009).

[22] C-S. Lee, E. Pop, A.D. Franklin, W. Haensch, H.-S. P. Wong: A Compact Virtual-Source Model for CarbonNanotube FETs in the Sub-10-nmRegime—Part I: Intrinsic Elements, *IEEE Transactions on Electron Devices*, **62**(9), 3061-3069, (2015).

[23] C-S. Lee, E. Pop, A.D. Franklin, W. Haensch, H.-S. P. Wong: A Compact Virtual-Source Model for CarbonNanotube FETs in the Sub-10-nm Regime—Part II:Extrinsic Elements, Performance Assessment,and Design Optimization, *IEEE Transactions on Electron Devices*, **62**(9), 3070-3078, (2015).

[24] R. Marani, A.G. Perri: Effects of Temperature Dependence of Energy Band Gap on I-V Characteristics in CNTFETs Models, *International Journal of Nanoscience*, **16**(0506), 1750009, (2017).
[25] G. Gelao, R. Marani, A.G. Perri: Effects of Temperature in CNTFET-Based Design of Analog Circuits, *ECS Journal of Solid State Science and Technology*, **7**(2), M16-M21, (2018).
[26] G. Gelao, R. Marani, A.G. Perri: Effects of Temperature in CNTFET-Based Design of Digital Circuits, *ECS Journal of Solid State Science and Technology*, **7**(3), M41-M48, (2018).
[27] G. Gelao, R. Marani, A.G. Perri: Effects of Temperature on Switching Time and Power Dissipation of CNTFET-Based Digital Circuits, *ECS Journal of Solid State Science and Technology*, **7**(4), M63-M68, (2018).
[28] R. Marani, G. Gelao, A.G. Perri: A Compact Noise Model for C-CNTFETs, *ECS Journal of Solid State Science and Technology*, **6**(4), pp. M118–M126, (2017).