CNTFET-BASED DESIGN OF DIGITAL CIRCUITS

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ABSTRACT
In this paper we implement a semi-empirical compact model for CNTFETs, already proposed by us, considering both the quantum capacitance effects and the sub-threshold currents in order to carry out static and dynamic analysis of basic digital circuits. To verify the validity of the obtained results, they are compared with those of Wong model, obtaining results in good agreement, but with a lighter ensuring compile and a shorter execution time.

Keywords: *CNTFET-based design, Modelling, Digital Circuits, CAD.*

1. INTRODUCTION

The evolution of electronics has been possible thanks to a scaling operation ever progressing with the time. This scaling evolution has been described by the Moore's law, which states that in an integrated circuit the number of transistors doubles every 18 months. However, today the scaling operation of silicon devices is saturated since these devices cannot be more shrunk without degrading their performances for the arising of some phenomena like tunnel effects [1] or the perforation of the gate oxide also for voltages relatively low. Therefore, the scientific community is looking for a new kind of devices, able to work better at nanometer scale, which is the new frontier.
Along with these new devices, molecular electronics will change the equation in our tool box, we will drop out well known partial differential equation for charge diffusion and we will use quantum mechanic to describe electrons, holes, atoms, molecules and photons. In coming years we will gain new tools from chemistry and physics, new sophisticated mathematical tool including probability amplitude waves.
Carbon NanoTube Field Effect Transistors (CNTFETs) are a new kind of molecular device and are regarded as an important contending device to replace conventional silicon transistors [2-3].
One of the major differences between CNTFETs and MOSFETs is that the channel of the devices is formed by Carbon NanoTubes (CNTs) instead of silicon, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon [2-3].
As it is known, the carbon nanotubes consist in a hexagonal mesh of carbon atoms wrapped in cylinder shapes, some time with closing hemispherical meshes on the tips. These tubes could have various radii, lower than two nanometers and, since they could be extended several millimeters, they have a huge length/diameter ratio making them unidimensional structures. Depending on the mesh torsion, denoted as *chirality*, electronic band structure of CNT changes, band gap may appear making them semiconductors, or may not appear, making them conductors [4-5].
Furthermore the CNT behaviour as semiconductor has an energy gap inversely proportional to their radius.
About modelling issues, the research on CNTFETs has proposed various models available in literature, which are numerical and make use of self-consistency and therefore they do not allow an easy implementation in circuit simulators (SPICE, Verilog-A or VHDL-AMS), which instead must be the main characteristic in the field of Computer Aided Design (CAD).
In our Refs. [6-13] we have already proposed a compact, semi-empirical model of CNTFET, in which we introduced some improvements to allow an easy implementation both in SPICE, using ABM library, and in Verilog-A.
In this paper we implement our CNTFET model to carry out static and dynamic analysis of basic digital circuits, obtaining results in good agreement with those of Wong model [14-15], but with a lighter ensuring compile and a shorter execution time.
The presentation is organized as follows. At first we briefly describe our compact, semi-empirical model of CNTFET, with reference to the main equations on which the CNTFET model is based.
Then we show the static and dynamic analysis of some logic gates and discuss the relative results, together with conclusions and future developments.

2. BRIEF ANALYSIS OF OUR CNTFET MODEL

2a) I-V Model

An exhaustive description of our model is in our Refs [2-7]. In this sub-Section we just describe the main equations on which our I-V model is based.

When a positive voltage is applied between drain-source ($V_{DS} > 0$ V), the hypothesis of ballistic transport [3] allows to assert that the current is constant along the CNT and therefore it can be calculated at the beginning of the channel, near the source, at the maximum of conduction band, where electrons from the source take up energy levels related to states with positive wave number, while the electrons from the drain take up energy levels related to states with negative wave number.

When a positive voltage is applied between gate-source ($V_{GS} > 0$ V), the conduction band at the channel beginning decreases by qV_{CNT}, where V_{CNT} is the surface potential and q is the electron charge. With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the drain current for every single sub-band can be calculated using the Landauer formula [16]:

$$I_{DSp} = \frac{4qkT}{h}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \tag{1}$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, ξ_{Sp} and ξ_{Dp} have the following expressions:

$$\xi_{Sp} = \frac{qV_{CNT} - E_{Cp}}{kT} \qquad \xi_{Dp} = \frac{qV_{CNT} - E_{Cp} - qV_{DS}}{kT} \tag{2}$$

being E_{Cp} the sub-bands conduction minima.

Therefore the total drain current can be expressed as:

$$I_{DS} = \frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \tag{3}$$

The surface potential, V_{CNT}, is evaluated by the following approximation [2]:

$$V_{CNT} = \begin{cases} V_{GS} & \text{for } V_{GS} < \dfrac{E_C}{q} \\ V_{GS} - \alpha\left(V_{GS} - \dfrac{E_C}{q}\right) & \text{for } V_{GS} \geq \dfrac{E_C}{q} \end{cases} \tag{4}$$

where E_C is the conduction band minima for the first sub-band.

The parameter α, depending on V_{DS} voltage, CNTFET diameter and gate oxide capacitance C_{ox}, has been extracted from the experimental device characteristics [1-3] and has the following expression [17]:

$$\alpha = \alpha_0 + \alpha_1 V_{DS} + \alpha_2 V_{DS}^2 \tag{5}$$

2b) C-V Model

An exhaustive description of our C-V model is widely described in our Refs. from 1 to 13 and therefore the reader is requested to consult it. Now we just describe the main equations on which is based our C-V model.

To determine the quantum capacitances C_{GS} and C_{GD}, it is necessary to know the total channel charge Q_{CNT}, having the following expression:

$$Q_{CNT} = q\sum_{p}\left(n_{Sp} + n_{Dp}\right) \tag{6}$$

where n_{Sp} and n_{Dp} are electron concentrations by the source and the drain respectively in the p-th sub-band. Having:

$$N_0 = \frac{4kT}{3\pi a_0|\gamma|} \tag{7}$$

where a_0 is the carbon-carbon (C-C) bonding distance (≈ 0.142 nm) and γ the C-C bonding energy (≈ 3 eV), the

number of carrier n_{ip} (i = S or D), which increases almost linearly as ξ_{ip} greater or equal than zero and falls off exponentially as ξ_{ip} becomes negative, can be derived from the following relationship [12]:

$$n_{ip} = N_0 \begin{cases} A_p \exp \xi_{ip} & \text{for } \xi_{ip} < 0 \\ B_p \xi_{ip} + A_p & \text{for } \xi_{ip} \geq 0 \end{cases} \qquad i = S, D \tag{8}$$

where the parameters A_p and B_p, depending on E_{Cp}, for $E_{Cp} < 0.5\,eV$, have the following empirical expressions [12]:

$$\begin{cases} A_p = -5.3E_{Cp}^2 + 10E_{Cp} + 1 \\ B_p = 0.34E_{Cp} + 1 \end{cases} \tag{9}$$

Therefore the quantum capacitances C_{GD} and C_{GS} are given by:

$$\begin{cases} C_{GD} = q\sum_p \frac{\partial n_{Dp}}{\partial V_{GS}} = q\sum_p \frac{\partial n_{Dp}}{\partial \xi_{Dp}} \frac{\partial \xi_{Dp}}{\partial V_{CNT}} \frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS} = q\sum_p \frac{\partial n_{Sp}}{\partial V_{GS}} = q\sum_p \frac{\partial n_{Sp}}{\partial \xi_{Sp}} \frac{\partial \xi_{Sp}}{\partial V_{CNT}} \frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \tag{10}$$

The CNTFET equivalent circuit, reported in Fig. 1, is similar to a common MOSFET and is characterized by the generator V_{FB}, for accounting the flat band voltage, and by the resistors R_D and R_S, in which the parasitic effect due to the electrodes are also included.

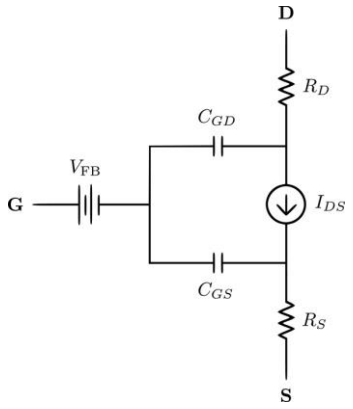

Figure 1. Equivalent Circuit of a n-type CNTFET [2-3].

Figures 2a and 2b show the implementation of the gate-drain and gate-source capacitances respectively using our C-V model in Verilog-A language [18], in which we have assumed V_{FB} = 0 V, CNT diameter d = 1.4 nm, $R_D = R_S = 0$ Ω and C_{ox} = 3.8 pF/cm.

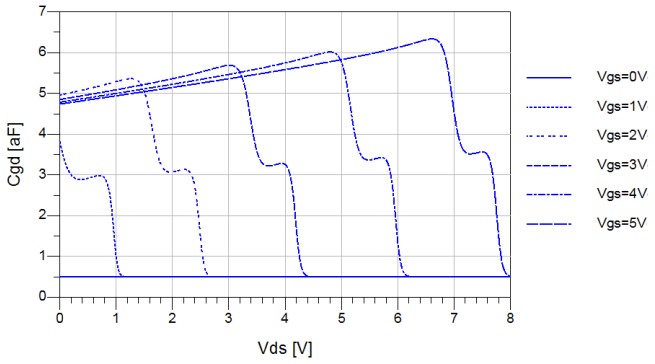

Figure 2a. Simulations of C_{GD} vs V_{DS} for different values of V_{GS} in Verilog-A.

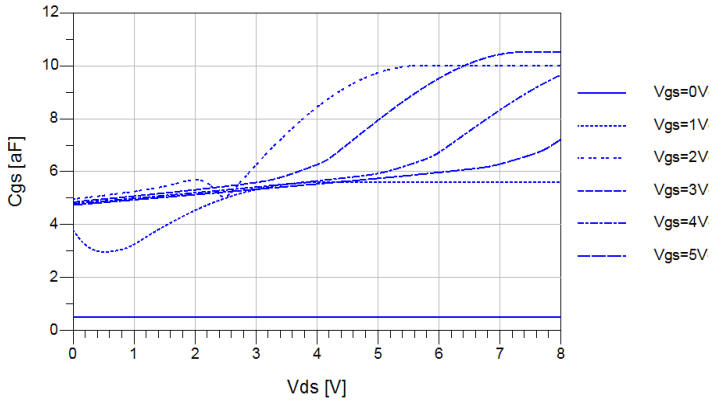

Figure 2b. Simulations of C_{GS} vs V_{DS} for different values of V_{GS} in Verilog-A.

The implementation of the same capacitances in SPICE has been reported in our Refs. 1 and 6, where we have obtained different values of gate-drain and gate-source capacitances, because in SPICE only one band in the capacitance model has been considered.
In particular, the difference between the capacitance models comes from some simplifications we have adopted in our SPICE model [6], in order to do not weigh down the software further, unlike Verilog-A implementation.
However these differences have no influence on I-V characteristics, which are practically the same, as illustrated previously.

3. STATIC ANALYSIS OF CNTFET LOGIC GATES

Referring to an inverter, for a static analysis we can determine the voltage transfer characteristic, VTC (Fig. 3), and then the noise margins, which provide a measure of the maximum external voltage noise that can be overlapped to the input signals, without causing unwanted output variation.
The noise margins, whose values are necessary in the design of digital circuits, are determined from the -1 slope points on the VTC, indicated by the letters A and B in Fig. 3, which delimit the amplification range of the device. V_{OH} and V_{IL} (point A) represent respectively the valid minimum output voltage at high level and the valid maximum input voltage at low level. Similarly V_{OL} and V_{IH} (point B) the valid maximum output voltage at low level and the valid minimum input voltage at high level.
The noise margins are defined as follows:
$NM_H = V_{OH} - V_{IH}$ for high voltage
and
$NM_L = V_{IL} - V_{OL}$ for low voltage.
When the input voltage V_I is between V_{IL} and V_{IH}, the logic gate is in an undefined state, which is an operative condition that we must avoid to make sure the logic levels are within well defined regions.

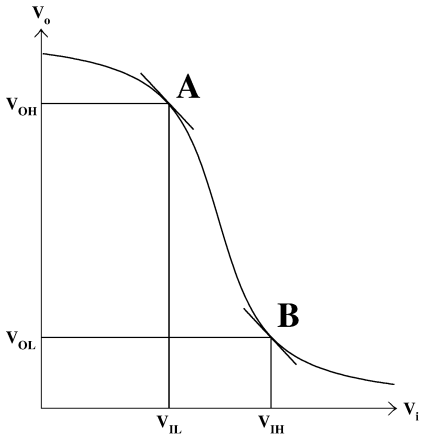

Figure 3. Voltage transfer characteristic for an inverter.

The schematic of NOT gate implemented by Verilog-A language is shown in Fig. 4.
The gate consists of two MOS-like CNTFETs with n and p channel respectively.
In Fig. 4 Gate-in and Out indicate the input and the output of the gate, while V+ and V- indicate the positive and negative power supply terminals. Two current probes have been introduced to evaluate static currents flowing through the two CNTFETs.
Finally, two capacitors have been introduced to model the capacitance of the metallic interconnections with respect to ground, which have no influence in static performance, but in dynamic analysis are important for new measurement technology.
In order to perform a static analysis, we have used the circuit reported in Fig. 5, which shows a cascade of five NOT gates, which are internally composed as in Fig. 4.
A dual power supply is used and a constant voltage source V_{in} is connected to the input of the first gate and varies from $-V_{CC}$ to $+V_{CC}$ (V_{CC} varies from 0.1V to 1V with step 0.1V).

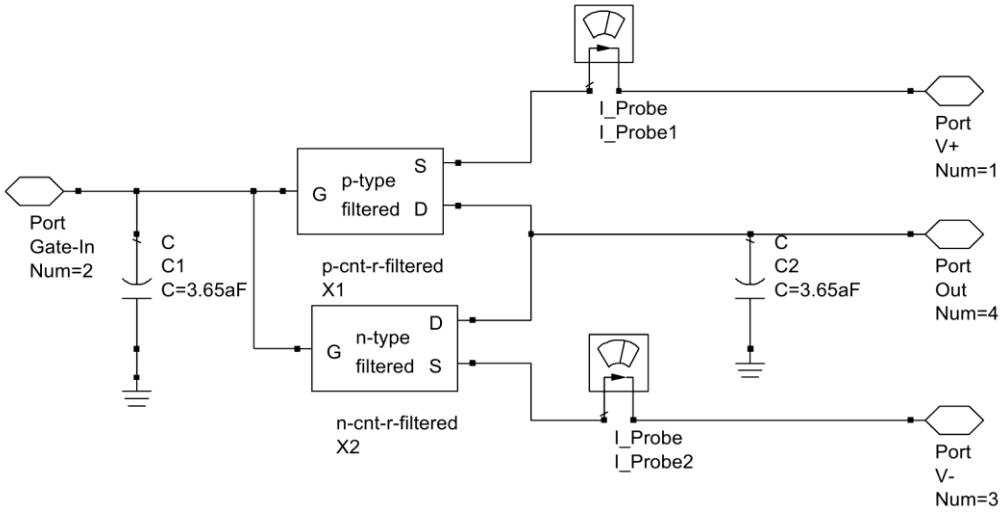

Figure 4. Schematic of a NOT gate.

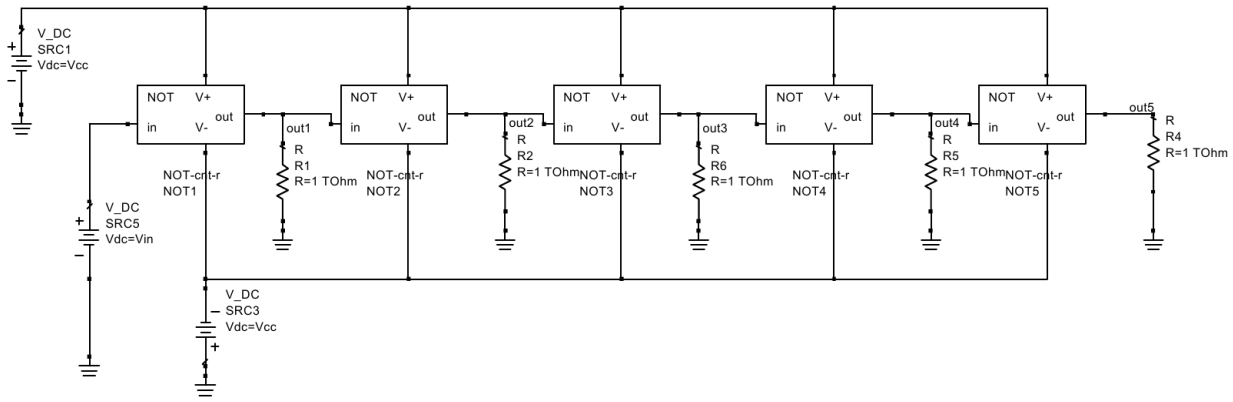

Figure 5. Schematic of a cascade of five NOT gates.

In Fig. 6 we have reported the simulated static currents of the first gate of the cascade. These currents give an indication of the static power dissipation in the circuit, which is a very important factor for high integration density circuits.

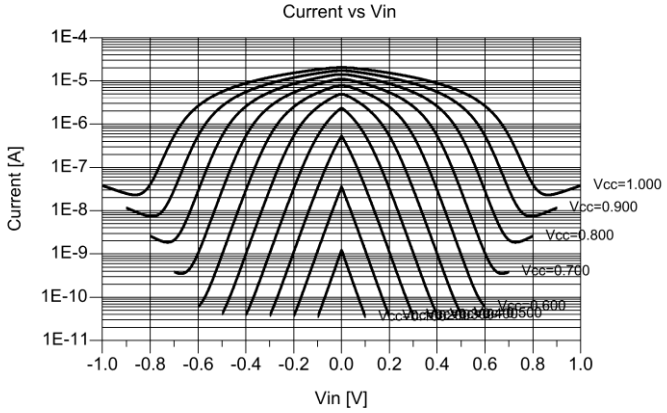

Figure 6. Static currents of the first NOT gate vs V_{in}, with V_{CC} varying from 0.1 V to 1.0 V.

Current peacks in the high gain region (near V_{in} = 0 V) are to be observed, because in this region the two CNTFETs of the NOT gate are both in the on state and they are saturated. A conducting path between the positive and negative power supply is determined and relatively high currents can flow. We can see that the current decreases in the regions where the gate state is well defined, i.e. the states where the input signal is recognized as low or high level. In these regions, where one transistor is turned on and the other one is turned off, the static current that flows between the positive and negative supply is due to the tunnel effect in the interdicted transistor.
As we said previously, noise margins are determined from the -1 slope points on the VTC. This slope is the gate gain and can be determined using the circuit of Fig. 7.

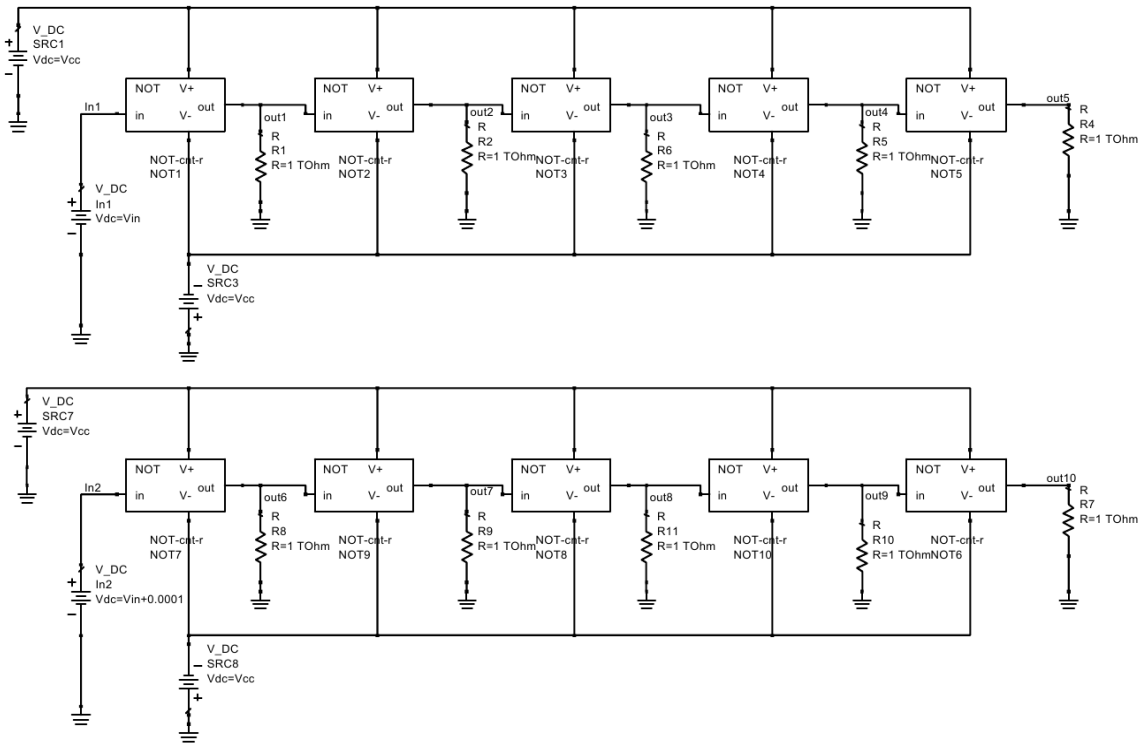

Figure 7. Circuit used to calculate NOT gain.

In particular Fig. 7 shows two identical circuits in which the lower one presents an input voltage increased by ΔV_{in} = 0.1mV with respect to the upper circuit. Referring to the first gate of the cascade, considering the difference between the outputs of the lower and upper circuit and dividing that by ΔV_{in} we obtain the gate gain.
Fig. 8 shows the gain diagrams of NOT1 gate as function of input voltage.

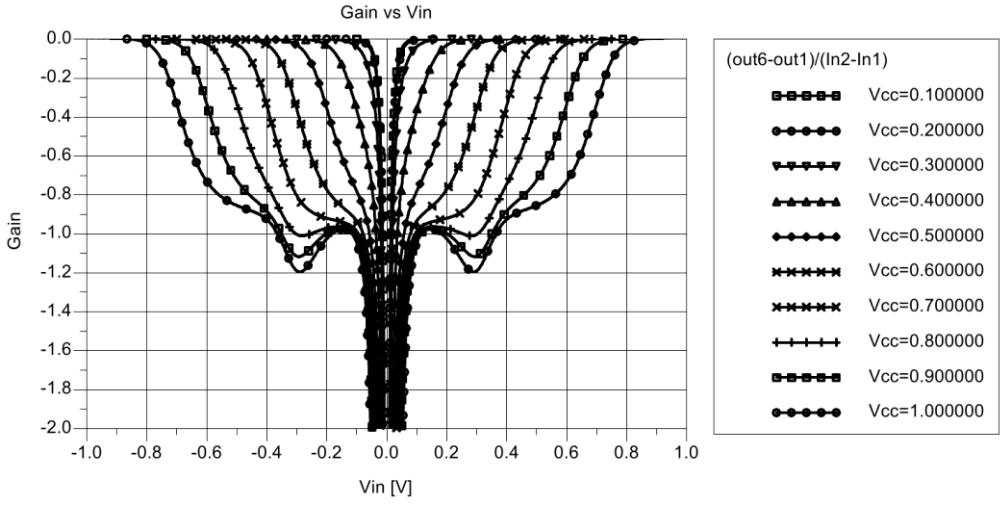

Figure 8. Gain of the first NOT of the cascade vs V_{in} with V_{CC} varying from 0.1 V to 1.0 V.

Similarly, plotting the gain as function of the output voltage of the first gate, we obtain V_{OH} and V_{OL}, which are the output voltage values when the gain is -1.
The results are shown in Fig. 9.

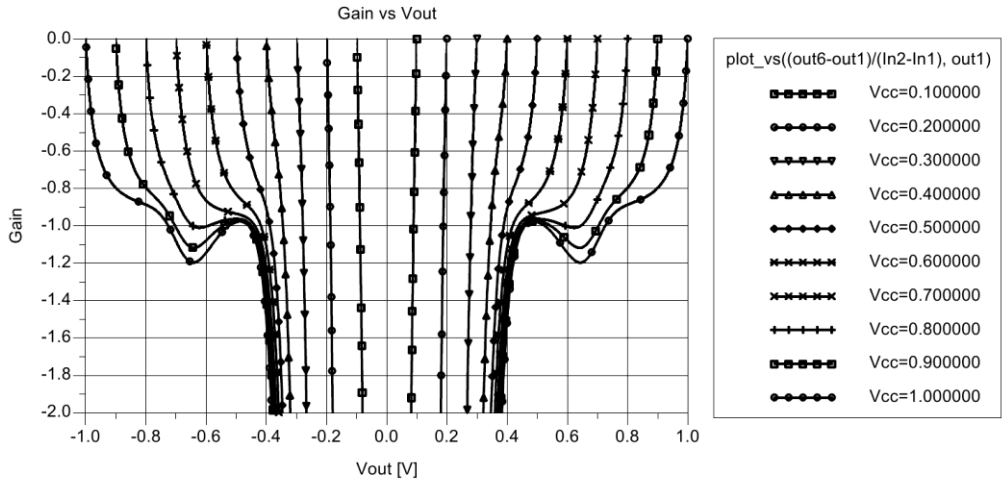

Figure 9. Gain of the first NOT of the cascade vs V_{out} with V_{CC} varying from 0.1 V to 1.0 V, step 0.1.

At last, in Table 1 we have reported the V_{IH}, V_{OL}, V_{IL}, V_{OH} values and the noise margins NM_H and NM_L for different values of V_{CC} for our model, whereas in Table 2 the same calculated using Wong model.

Table 1. Noise margins and -1 slope points (our model).

V_{CC} [V]	V_{IH}[V]	V_{OL}[V]	V_{IL}[V]	V_{OH}[V]	NM_H	NM_L
0,1	0,014	-0,089	-0,014	0,089	0,075	0,075
0,2	0,014	-0,188	-0,014	0,188	0,174	0,174
0,3	0,019	-0,278	-0,019	0,278	0,259	0,259
0,4	0,0357	-0,345	-0,0357	0,345	0,3093	0,3093
0,5	0,0578	-0,388	-0,0578	0,388	0,3302	0,3302
0,6	0,076	-0,419	-0,076	0,419	0,343	0,343
0,7	0,095	-0,439	-0,095	0,439	0,344	0,344

Table 2. Noise margins and -1 slope points (Wong model)

V_{CC} [V]	V_{IH}[V]	V_{OL}[V]	V_{IL}[V]	V_{OH}[V]	NM_H	NM_L
0,1	0,018	-0,088	-0,018	0,088	0,07	0,07
0,2	0,0195	-0,185	-0,0195	0,185	0,1655	0,1655
0,3	0,0325	-0,265	-0,0325	0,265	0,2325	0,2325
0,4	0,0535	-0,325	-0,0535	0,325	0,2715	0,2715

In all following simulations we have considered CNTFETs having a diameter of 1.42 nm, length of 100 nm and quantum capacitances depending on polarization voltages.

4. DYNAMIC ANALYSIS OF CNTFET LOGIC GATES

To analyze the dynamic behaviour of a logic gate, for example an inverter, the parameters of interest are the propagation delay and the rise and fall times (see Fig.10).

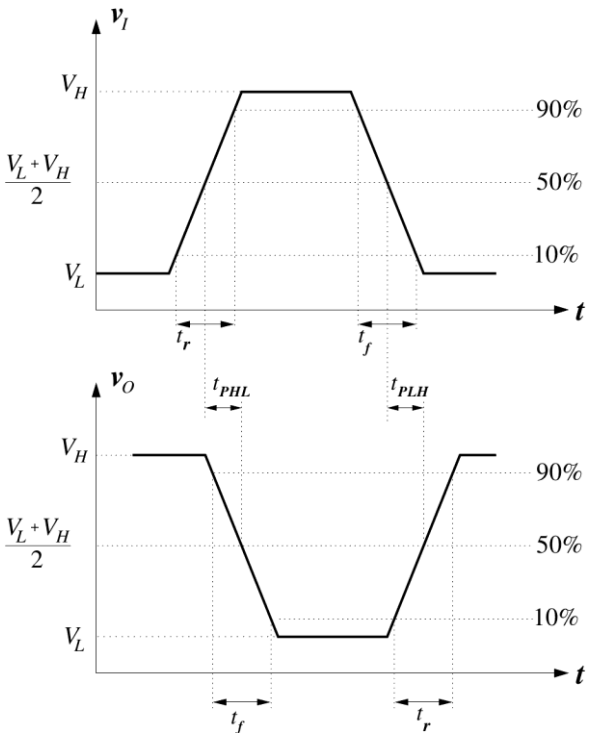

Figure 10. Time and voltage definitions for input and output waveforms [19].

The rise time t_r for a given signal is defined as the time required for the signal to make the transition from the 10% point to the 90% point on the waveform, during the V_L-V_H transition.
Similarly, the fall time t_f is defined as the time required for the signal to make the transition between the 90% point and the 10% point on the waveform, during the V_H-V_L transition.
The 10% and 90% points are defined as follows:
$V_{10\%} = V_L + 0.1\Delta V$
$V_{90\%} = V_L + 0.9\Delta V$
where $\Delta V = V_H - V_L$ is the logic swing, V_H and V_L are the high and low logic levels respectively.
The **propagation delay τ_P** is defined as the difference in time between the input and output signals reaching the 50% points in their respective transitions. The 50% point is the voltage level corresponding to one-half the total transition between V_H and V_L: $V_{50\%} = (V_H + V_L)/2$
We indicate propagation delay on the high-to-low output transition with τ_{PHL} and that of the low-to-high transition with τ_{PLH}.
The schematic of NOT gate implemented by Verilog-A language has been already shown in Fig. 4.
In order to perform a dynamic analysis, we have used the circuit reported in Fig. 5, already illustrated.
Parasitic capacitors have been introduced on the outputs of the gates to model the capacitance to ground of the metallic interconnections between gates. The input of the first gate is connected to an impulsive voltage generator that provides a binary signal with high level equal to $+V_{CC}$ and low level equal to $-V_{CC}$, rise and fall times equal to 1.78 ps (**slow transitions**), high level duration of 16 ps and period equal to 38 ps. The rise and fall times have been chosen to give in input a typical signal of the logic, with features similar to the output signal of the cascade. For the following simulations we use a voltage supply V_{CC} = 0.4V, which determines the values of the high and low logic levels. In particular we chose a simulation time equal to 80 ps that allows to view the complete waveforms at the outputs of the gates.
Fig. 11 shows the result of simulation for slow transitions for our model.

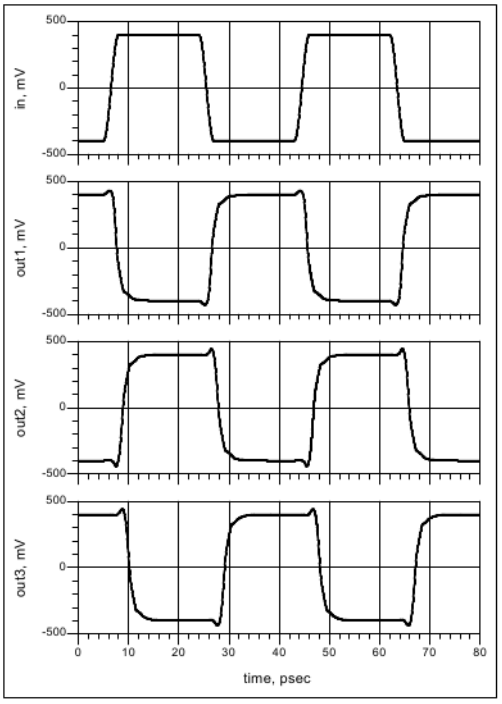

Figure 11. Output of the first four NOT gates and input signal vs time for slow transitions.

Figures 12 and 13 allow to determine the propagation delays for the high-to-low and low-to-high transitions respectively.

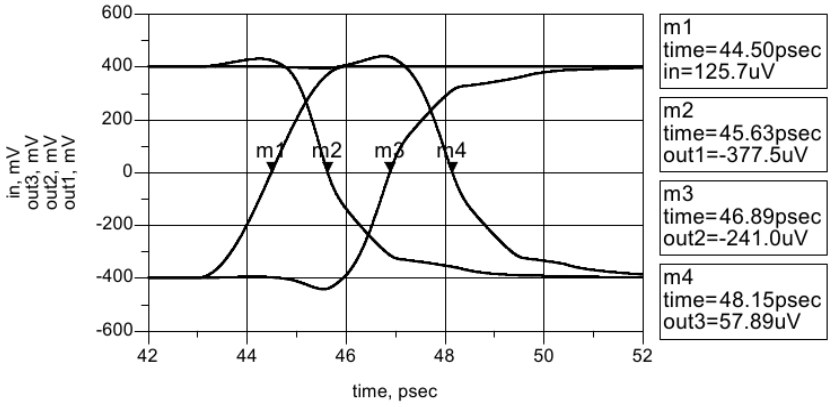

Figure 12. Input and output of transients of the NOT gates for high-to-low transitions.

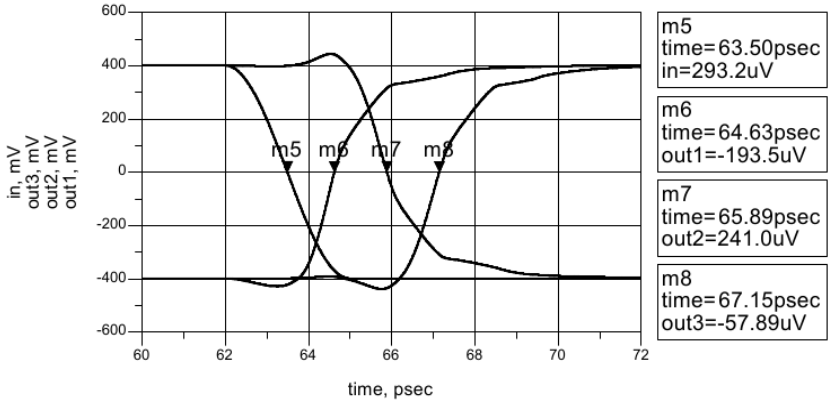

Figure 13. Input and output of transients of the NOT gates for low-to-high transitions.

On these diagrams we have superposed some markers in order to determine the times corresponding to the 50% points of the transitions. The 50% points are equal to 0 V. In this way we can easily determine the propagation delays τ_{PHL} and τ_{PLH}, applying the definitions mentioned before. For example, for the first NOT gate we obtain:

$\tau_{PHL1} = t_{m2} - t_{m1} = 45.63 \text{ ps} - 44.50 \text{ ps} = 1.13 \text{ ps}$

$\tau_{PLH1} = t_{m6} - t_{m5} = 64.63 \text{ ps} - 63.50 \text{ ps} = 1.13 \text{ ps}$

Moreover Figs. 14 and 15 allow to evaluate the rise and fall times of the input and output signals at the first NOT of the cascade respectively.

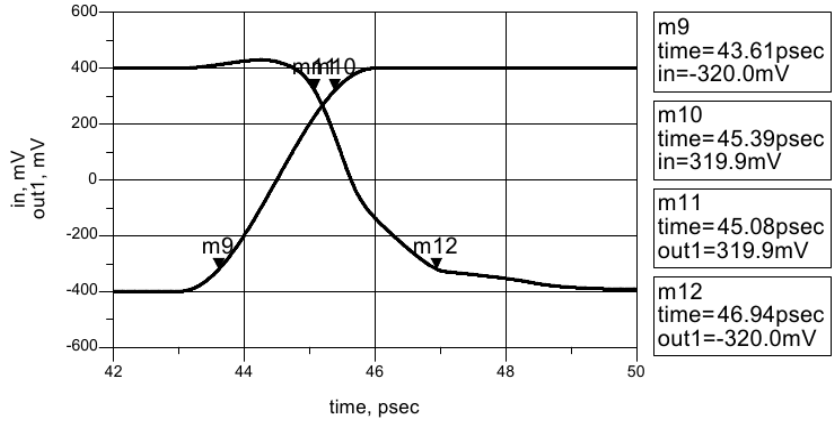

Figure 14. Input and output of transients of the first NOT gate for high-to-low transitions.

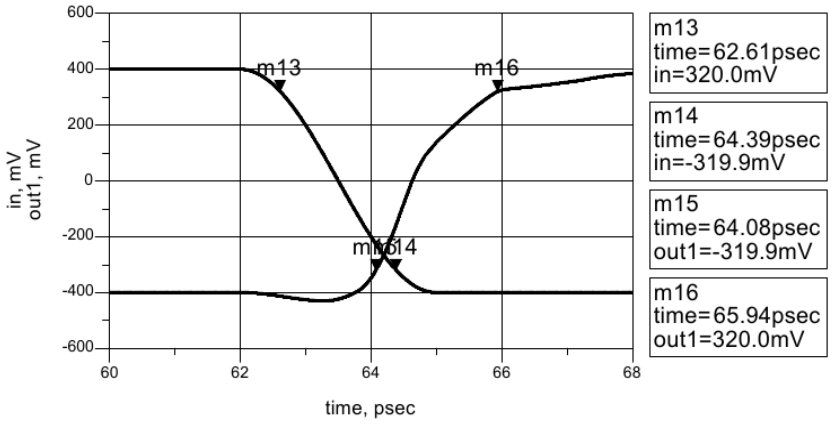

Figure 15. Input and output of transients of the first NOT gate for low-to-high transitions.

The markers on the diagrams have been positioned at the 10% and 90% points of the level transition: in this way it is possible to determine easily the rise times t_r and the fall times t_f in the following way:

$V_{10\%} = V_L + 0.1\Delta V = -400 \text{ mV} + 0.1 \cdot 800 \text{ mV} = -320 \text{ mV}$

$V_{90\%} = V_L + 0.9\Delta V = -400 \text{ mV} + 0.9 \cdot 800 \text{ mV} = 320 \text{ mV}$

where $\Delta V = V_H - V_L = 400 \text{ mV} - (-400 \text{ mV}) = 800 \text{ mV}$

Corresponding to the markers, it is possible to read the times referring to these points and, therefore we can determine the rise times t_r and the fall times t_f. which refer to the input and output signals.

For example, for the first gate:

$t_{r1} = t_{m12} - t_{m11} = 47.43 \text{ ps} - 45.15 \text{ ps} = 2.28 \text{ ps}$

$t_{f1} = t_{m16} - t_{m15} = 66.43 \text{ ps} - 64.15 \text{ ps} = 2.28 \text{ ps}$

In order to evaluate the dynamic currents due to not instantaneous transition of the input signal of the gate, it is necessary observe that, during the level transition of the input signal, for a short time, both the CNTFETs are saturated. This happens when the signal leads the gate to the transition region. Therefore, a conducting path between the positive and negative supply exists and a certain current can flow through that path.

Performing the simulation for the first NOT of the cascade using our model we obtain the diagram shown in Fig. 16, while, for Wong model, we obtain the result shown in Fig. 17.

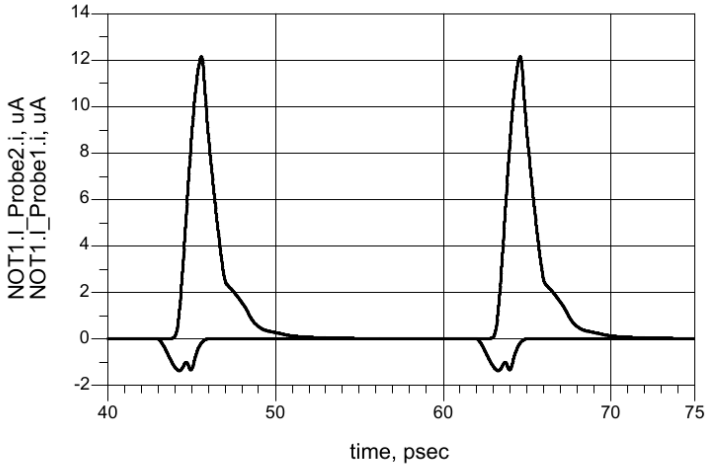

Figure 16. Dynamic currents flowing through the first NOT gate (our model).

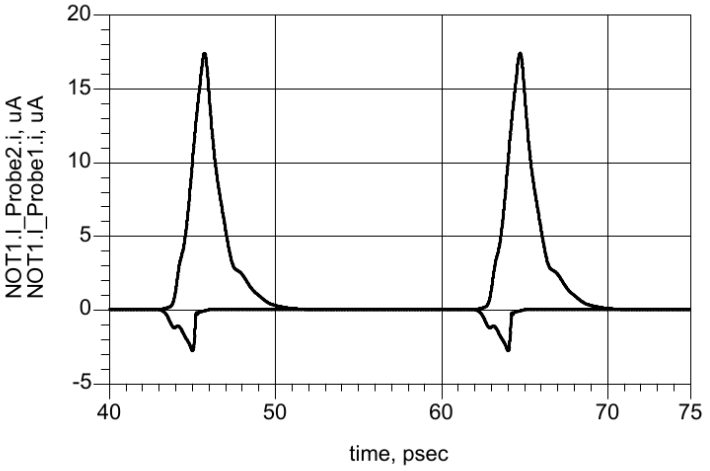

Figure 17. Dynamic currents flowing through the first NOT gate (Wong model).

In both figures the n-channel CNTFET current corresponds to the first positive peak, while the p-channel CNTFET current corresponds to the first negative peak. The situation is inverted for the current peaks at 65 ps.
When the input signal at the first gate passes from the low level to the high level, the p-CNTFET turns off, whereas the n-CNTFET turns on. The load capacitance on the output of the gate, initially at high voltage level, discharges through the n-CNTFET, turned on, determining a current peak through this device which lasts for the time necessary to discharge the capacitance.
Similarly, when the input signal at the first gate passes from the high level to the low level, the n-CNTFET turns off, whereas the p-CNTFET turns on. The load capacitance starts to charge through the p-CNTFET, therefore the output passes from the initially low level to the high level, at the end of the transient. The current peak, in this case, flows through the p-CNTFET and lasts for the time necessary to charge the load capacitance.
We have repeated the proposed procedure to analyze the dynamic behaviour of NOR gate, but, in order not to weigh the treatment, we limit ourselves to report the obtained results in Table 3.

Table 3. Results of the transient analysis of the NOR cascade for fast transitions.

Time (ps)	**Our Model**	**Wong Model**
τ_{PHL1}	2.14	2.35
τ_{PLH1}	3.72	4.51
t_{r1}	8.91	9.83
t_{f1}	4.58	4.91

For the transient analysis, the differences observed on the results of the two models are mainly due to the different implementation of the internal capacitances of the CNTFET.
All simulations were carried out in ADS on an Asus X5DIJ computer which uses an Intel Pentium dual core T4200 processor running at 2 GHz, with 1 MB cache and 4 GB of RAM memory. Moreover we have obtained a compilation time of 2.69 s and a run time of 58.84, while, using the Wong model, the values have been of 47.70 s and 1336.42 s respectively.

5. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper we have improved the semi-empirical compact model for CNTFETs already proposed by us, considering both the quantum capacitance effects and the sub-threshold currents in order to carry out dynamic analysis of basic digital circuits.
To verify the validity of the obtained results, they have been compared with those of Wong model [14-15] using for this model the version downloadable on website of Stanford University, which, up today, refers to the model published in Refs. 20 and 21, obtaining a lighter ensuring compile and shorter execution time, which are the main model characteristics to obtain an easy implementation in circuit simulators.
Actually we are working to study the effect of noise [22] and of temperature [23-24] in the CNTFET-based design of A/D circuits.

6. REFERENCES

[1] A.G. Perri, R. Marani: CNTFET Electronics: Design Principles, Ed. Progedit. Bari, Italy, ISBN:978-88-6194-307-0, (2017).
[2] A.G. Perri, Fondamenti di Dispositivi Elettronici *Avanzati*, Ed. Progedit, Bari, Italy, ISBN 978-88-6194-080-2, **(**2016).
[3] A.G. Perri, Dispositivi Elettronici Avanzati, Ed. Progedit, Bari, Italy, ISBN 978-88-6194-081-9, (2016).
[4] R. Marani, A.G. Perri, Modelling the Electronic Characteristics of Carbon Nanotubes, *Proceedings of 1st Transalp'Nano Conference*, Lyon, France, (2008).
[5] R. Marani, A.G. Perri: CNTFET Modelling for Electronic Circuit Design, *ElectroChemical Transactions*, **23**(1), 429-437, (2009).
[6] G. Gelao, R. Marani, R. Diana, A.G. Perri: A Semi-Empirical SPICE Model for n-type Conventional CNTFETs, *IEEE Transactions on Nanotechnology*, **10**(3), 506-512, (2011).
[7] R. Marani, A.G. Perri: A Compact, Semi-empirical Model of Carbon Nanotube Field Effect Transistors oriented to Simulation Software, *Current Nanoscience*, **7,**(2), 245-253, (2011).
[8] R. Marani, A.G. Perri: A DC Model of Carbon Nanotube Field Effect Transistor for CAD Applications, *International Journal of Electronics*, **99**(3), 427-444, (2012).
[9] R. Marani, G. Gelao, A.G. Perri: Comparison of ABM SPICE library with Verilog-A for Compact CNTFET model implementation!, *Current Nanoscience*, **8**(4), 556-565, (2012).

[10] R. Marani, G. Gelao, A.G. Perri: Modelling of Carbon Nanotube Field Effect Transistors oriented to SPICE software for A/D circuit design, *Microelectronics Journal*, DOI:10.1016/j.mejo.2011.07.012, 33-39, (2013).
[11] R. Marani, A.G. Perri: Analysis of CNTFETs Operating in SubThreshold Region for Low Power Digital Applications, *ECS Journal of Solid State Science and Technology*, **5**(2), M1-M4, (2016).
[12] R. Marani, A.G. Perri: A Simulation Study of Analogue and Logic Circuits with CNTFETs, *ECS Journal of Solid State Science and Technology*, **5**(6), M38-M43, (2016).
[13] R. Marani, A.G. Perri: A Comparison of CNTFET Models through the Design of a SRAM Cell, *ECS Journal of Solid State Science and Technology*, **5**(10), M118-M126, (2016).
[14] C-S. Lee, E. Pop, A.D. Franklin, W. Haensch, H.-S. P. Wong: Compact Virtual-Source Model for Carbon Nanotube Field Effect Transistors in the Sub-10-nm Regime—Part I: Intrinsic Elements, *IEEE Transactions on Electron Devices*, **62**(9), 3061-3069, (2015).
[15] C-S. Lee, E. Pop, A.D. Franklin, W. Haensch, H.-S. P. Wong: A Compact Virtual-Source Model for Carbon Nanotube FETs in the Sub-10-nm Regime—Part II: Extrinsic Elements, Performance Assessment, and Design Optimization, *IEEE Transactions on Electron Devices*, **62**(9), 3070-3078, (2015).
[16] S. Datta, Cambridge Studies in Semiconductor Physics and Microelectronic Engineering 3. New York: Cambridge University Press, ISBN 978-0-521-599943-6, (1995).
[17] A. Raychowdhury, S. Mukhopadhyay, K. Roy: A circuit-compatible model of ballistic carbon nanotube field-effect transistors, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **23**(10), 1411-1420, (2004).
[18] Verilog-AMS language reference manual, Version 2.2, Accellera International, Inc., (2006).
[19]A. G. Perri: Fondamenti di Elettronica, Ed. Progedit, Bari, Italy, ISBN 978-88-6194-045-1, **(**2009).
[20] J. Deng, H.-S. P. Wong: A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region", *IEEE Transactions on Electron Devices*, **54**(12), 3186-3194, (2007).
[21] J. Deng, H.-S. P. Wong: A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking, *IEEE Transactions on Electron Devices*, **54**(12), 3195-3205, (2007).
[22] R. Marani, G. Gelao, A.G. Perri: A Compact Noise Model for C-CNTFETs, *ECS Journal of Solid State Science and Technology*, **6**(4), M118-M126, (2017).
[23] R. Marani, A.G. Perri: Effects of Temperature Dependence of Energy Band Gap on I-V Characteristics in CNTFETs Models, *International Journal of Nanoscience*, **16**(05-06), doi:10.1142/S0239581X17500090, (2017).
[24] R. Marani, A.G. Perri: A DC Thermal Model of Carbon Nanotube Field Effect Transistors for CAD Applications, *ECS Journal of Solid State Science and Technology*, **5**(8), M3001-M3004, (2016).