EFFECT OF SUBSTRATE DOPING CONCENTRATION ON ELECTRICAL CHARACTERISTICS OF LDD MOSFET DEVICES

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ABSTRACT
In this paper we present the effect of variation of substrate doping concentrations on I-V characteristics of Lightly Doped Drain (LDD) MOSFETs through a simulation study applicable also to any submicron device. The used software is TCAD simulator, which provide general capabilities for numerical, physically-based, two-dimensional simulation of semiconductor processing.
At last we examine a linear model, in which we propose an appropriate approximation, that allows to simulate more adequately the effects of variation of the process parameters as correction to the base model of the device.

Keywords: *LDD MOSFET Devices, Drain Engineering, Modelling, Device Simulations.*

1. INTRODUCTION

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), having sub-micrometer dimensions, present, near the active regions of the device, a high electric field in order to keep the supply voltage constant, causing the well-known effect called hot carrier effect. The hot carriers enter in the oxide layer, accumulating over time. This accumulation degrades the device performances, producing a reduction of device lifetime and increasing the threshold voltage V_T [1-3]. To prevent the phenomenon of hot carriers it necessary to act at the drain (drain engineering) where we have the highest value of electric field (and likewise at the source).
The most well-known structure used to reduce the electric field is the Lightly Doped Drain (LDD) structure [4-13], which has higher breakdown voltage, lower electric field near the source and drain regions and lower gate current, that make it suitable for submicron devices. The LDD structure can be applied to non-silicon-based devices such as graphene nanoribbon field effect transistors (GNRFETs) [14]. Actually numerous other structures have been proposed in order to reduce the electric field inside the structure [15].
However one of the most important disadvantages for LDD structure is an increased output resistance [16], which degrades current capability of the device [17]. This problem can be alleviated designing the LDD architecture having appropriate values of substrate doping concentration. Since electrons in Si have a higher mobility than holes, n-channel devices are more negatively influenced by the effect of high electric field resulting in a greater number of hot-electrons injected into the gate oxide [18]. For this reason, we study a LDD structure for n- type MOSFETs.
In this paper we present the effect of variation of substrate doping concentrations on I-V characteristics of LDD MOSFETs through a simulation study. However the proposed study can be applied also to any submicron device [19-20].
In particular we show the effect on the output impedance, on the trans-conductance and on threshold voltage of the examined device.
The presentation is organized as follows. At first we briefly describe the Lightly Doped Drain MOSFET structure. Then we show the effect of variation of substrate doping concentrations on simulated I-V characteristics of LDD MOSFET, discussing the relative results, together with conclusions and future developments..

2. BRIEF ANALYSIS OF LDD DEVICE

In the Lightly Doped Drain technique (LDD), the drain region (and source) is formed with a first diffusion more extended of atoms at concentration N-, and then with a second diffusion at concentration N+ less extensive, but deeper. The effect is always to provide a gradual doping profile of the drain region (and source) so as to reduce the maximum electric field [1-3].

From [3] we can see that the value of breakdown voltage obtained for LDD MOSFET is double than the same value for conventional MOSFET. This happens because hot electrons near drain and source are slowed down since electric field near active regions is decreased by the presence of light doping. The breakdown voltage is proportionally with the radius of source/drain junctions. N-channel length has also an important influence on breakdown voltage. If channel dimensions are small, then the current flowing through channel has to travel over a shorter distance between source and drain. In this way current capability of the device is increased: small resistance and greater current. On the other hand, shorter channel makes breakdown voltage smaller due to unideal scaling, the internal electric field would increase with shorter channel lengths [2].

The reduction in electric-field intensity due to the LDD structure is illustrated in the two-dimensional simulation results reported in [21], where it is possible to see that the electric field in the conventional device peaks approximately at the metallurgical junction and drops quickly to zero in the drain because no field can exist in the highly conductive N+ region. On the other hand, the electric field in the LDD device extends across the N- region before dropping to zero at the drain. For a given voltage drop the peak field in the LDD device, which determines the junction avalanche breakdown voltage, is lower than in the conventional device.

In this paper the LDD performances are studied on a MOSFET device using TCAD simulator [22], containing process and device simulation modules.

The LDD MOSFET under investigation has been realized on Silicon substrate with <100> crystallographic orientation and an initial doping with phosphor atoms of 10^{14} cm^{-3} . The P-well region is obtained implanting a dose of boron atoms of $8 \cdot 10^{12}$ cm^{-2} with 100 keV of energy. Source and drain regions are obtained with a dose of arsenic implant of $2.5 \cdot 10^{15}$ cm^{-2} and 50 keV energy with polysilicon gate as mask. LDD implants are made with a dose of phosphor atoms of $3 \cdot 10^{13}$ cm^{-2} with 20 keV of energy.

The aim of this paper is the study of the effect of substrate doping on electrical characteristics. In particular we examine different dose of boron atoms for the P-well region in order to determine the optimal value of substrate doping.

3. EFFECT OF DOSE IMPLANTATION IN P-WELL REGION ON I_{DS}-V_{DS} CHARACTERISTICS

In this section we would examine the effect of variation of boron dose (from $8 \cdot 10^{9}$ cm^{-2} to $8 \cdot 10^{13}$ cm^{-2}) in the P-Well region on Ids-Vds characteristics for three different gate voltage (1.1V, 2.2V, 3.3V). The boron energy is fix at 100 KeV.

In particular we plot the output characteristic on a large interval of Vgs (gate-source voltage) and Vds (drain-source voltage) in order to show better the trends of the variation on these characteristics.

Figures 1 and 2 show the Ids-Vds behaviour for Vds from 0 to 10 V using a boron dose equal to $8 \cdot 10^{12}$ cm^{-2} and $8 \cdot 10^{13}$ cm^{-2} respectively.

We use this range for Vds in order to see the high-voltage effects as well. In this range we can affirm that there is no breakdown effect for the proposed LDD MOSFET.

Moreover we can see a fall in the current while the dose of implantation increases. As it can seen in Fig. 2 for Vgs set at 1.1 V, the drain current is equal to zero, because the threshold voltage of LDD MOSFET grows with the dose of implantation.

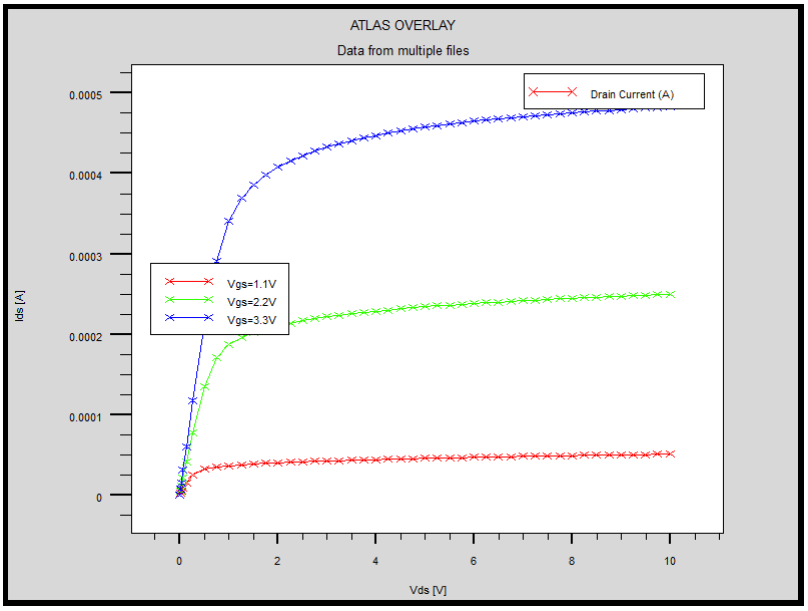

Figure 1. Ids-Vds characteristics using a boron dose 8·10^{12} cm^{-2}.

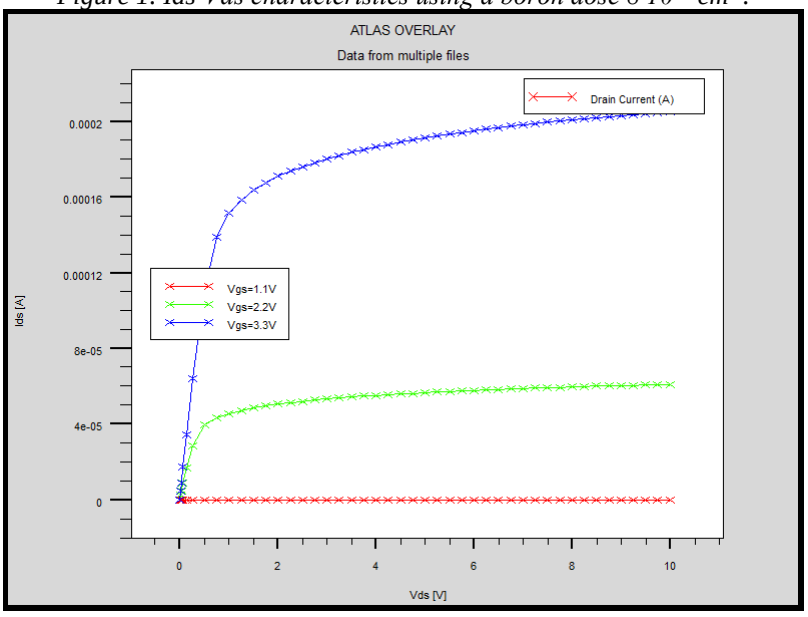

Figure 2. *Ids-Vds characteristics using a boron dose 8·10^{13} cm^{-2}.*

Now we would examine the effect on Ids-Vds characteristics when the boron dose decreases.
The results of simulations for boron dose of implantation of 8·10^{11} cm^{-2}, 8·10^{10} cm^{-2} and 8·10^{9} cm^{-2} are shown in Figures 3, 4, and 5 respectively.

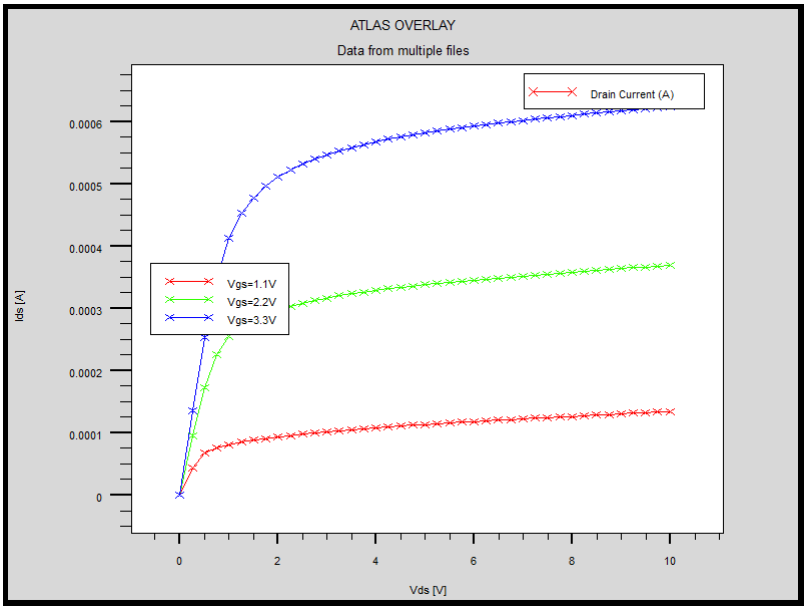

Figure 3. Ids-Vds characteristics using a boron dose 8·10^{11} cm^{-2}.

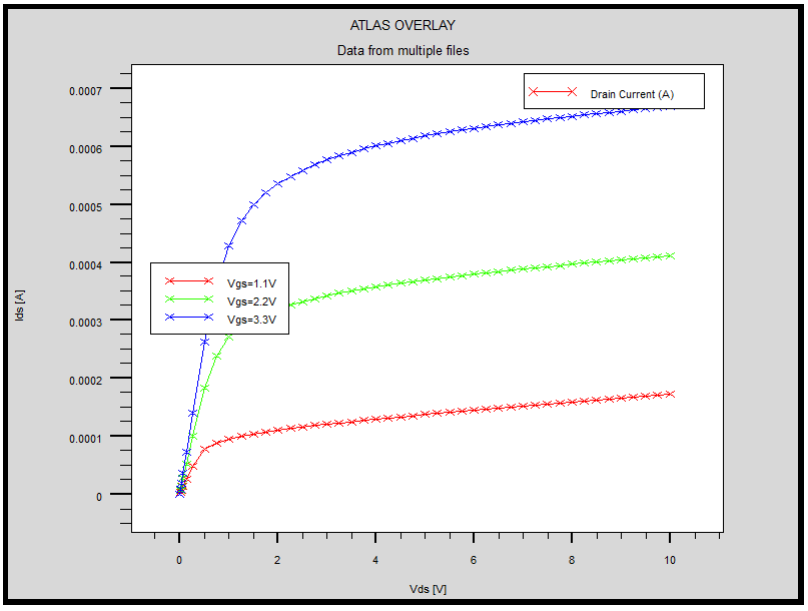

Figure 4. Ids-Vds characteristics using a boron dose $8 \cdot 10^{10}$ cm^{-2}.

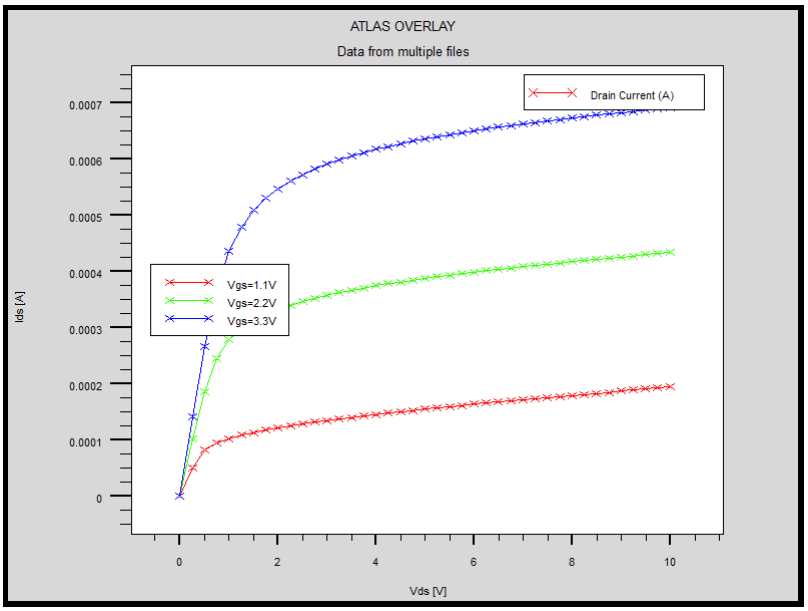

Figure 5. Ids-Vds characteristics using a boron dose $8 \cdot 10^{9}$ cm^{-2}.

We can summarize all these characteristics with Fig. 6 which shows the Ids current for different boron implantation doses (Vgs value is set to 1.1 V).

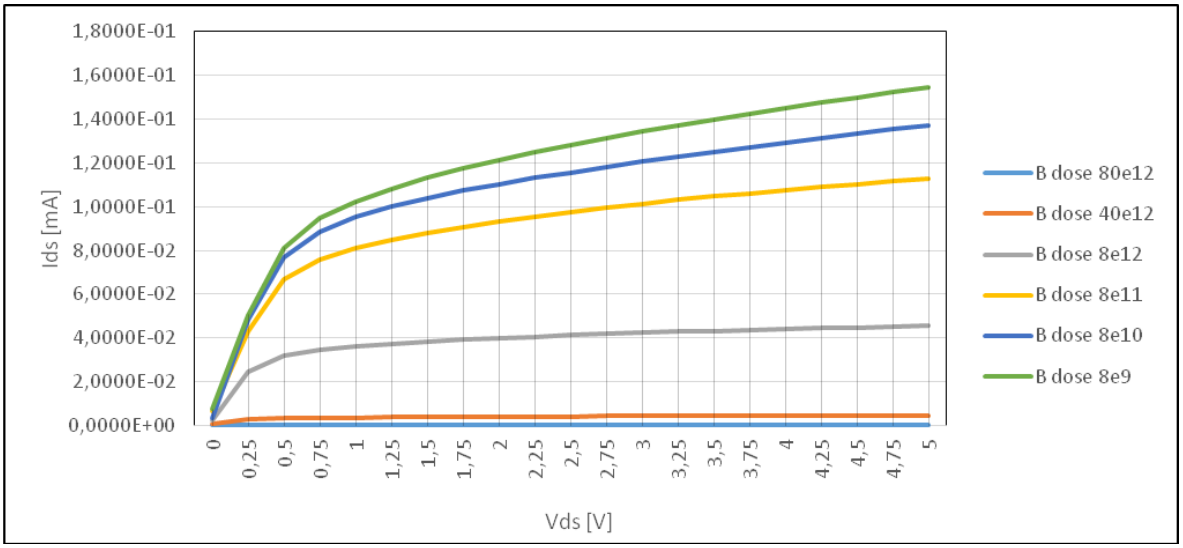

Figure 6. Ids-Vds characteristics using the considered boron doses for Vgs = 1.1 V.

Fig. 6 allows to affirm that Ids increases while the implantation dose increases, while, for $8 \cdot 10^9$ cm^{-2}, the LDD device is below the threshold voltage and therefore the current is almost null.
In Fig. 7 we plot the value of output resistance versus Vds for each boron dose considered. The simulation values of Fig. 7 are extracted using MATLAB software (23).

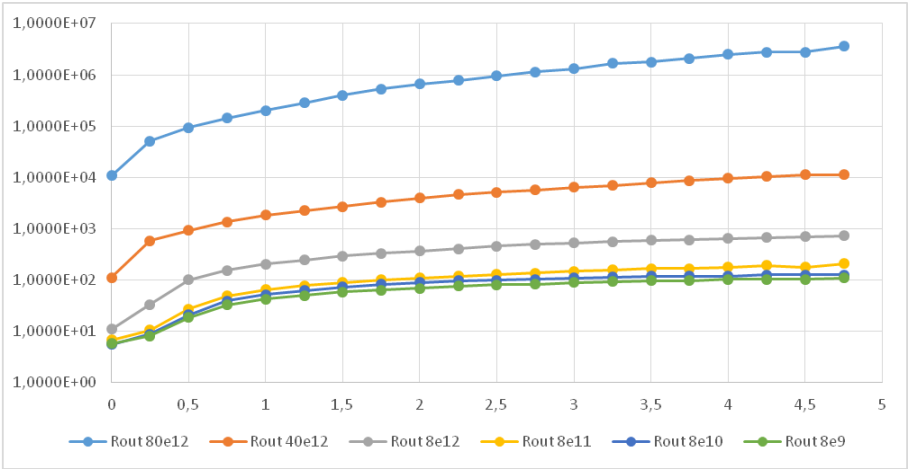

Figure 7. Rout-Vds characteristics using the considered boron doses for Vgs = 1.1 V.

As expected Rout increases when boron dose decreases.

4. DISCUSSION OF RESULTS

The analysis of the variations of Ids due to the variation of substrate doping concentrations shows patterns specific to the fabrication parameters.
Modern tools allow to simulate variability and some correlation of the variability, since they work on variation of model parameters but hardly they would present pattern of the variation as those we found.
When we fit a model on the base data (i.e. those without variations), we obtain a fit quite satisfactory for general applications, but usually it is not so stick to the data to sense correctly the Ids-Vds variation due to fabrication process. Indeed when the model is fitted to the altered Ids-Vds data, the fitting procedure senses both the data variation and the inadequacy of the model, and therefore it is not possible to represent in an appropriate way the effect of the process variation using the model parameters. We observed this problem, fitting a model on the simulated data for different process parameter variations.

In the light of the obtained results, we propose a I-V model where we use the variation patterns as base for the variability of the device:

$$I_D(V_{GS}, V_{DS}) = I_D^0(V_{GS}, V_{DS}) + \sum_P \left(\frac{\partial I_D(V_{GS}, V_{DS})}{\partial P} * \delta P \right) \quad (1)$$

where I_D^0 is the base model and δP is the variation of the fabrication parameter P. Moreover we approximate:

$$\frac{\partial I_D(V_{GS}, V_{DS})}{\partial P} \approx \frac{\Delta I_D(V_{GS}, V_{DS})}{\Delta P} \quad (2)$$

i.e. the derivate with the variation ratio obtained by device simulations for a specified value of parameter P (in this paper P is the variation of substrate doping concentrations).
Eq. (2) can be implemented as look-up tables or as a functional approximation. In this way the effect of the variation of process parameters could be simulated more adequately as correction to the base model.

5. CONCLUSION AND FUTURE DEVELOPMENTS

In this paper we have simulated the effect of variations of process parameters on output I-V characteristics of LDD MOSFET. In particular we have examined the effect of variation of substrate doping concentrations through a simulation study applicable also to any submicron device.
The results obtained are coherent with theory: in fact we have shown that the threshold voltage increases with the dose of implantation, but output resistance decreases. Therefore, in the design of the LDD structure, it is necessary a trade-off to be made between output resistance and threshold voltage itself, depending on the type of applications.
At last we have examined a linear model, in which we have proposed an appropriate approximation, that allows to simulate more adequately the effects of variation of the process parameters as correction to the base model of the device.
Nowadays the continuous need to have littler and faster consumer devices such as laptops, smart-phones, cameras and so on, drive companies to develop smaller and smaller electronic components. Si technology almost reached its physical limits and a further scaling is practically impossible. A new kind of technology, based on Carbon NanoTube (CNT), seems to satisfy the market demand and the need to scaling all the electronic components [24-35]. Currently we are studying these new devices.

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