VOLTAGE BALANCING CONTROL STRATEGY IN CONVERTER SYSTEM FOR THREE-LEVEL INVERTERS

Srinivas Dasam[1,*], B.V. Sanker Ram[2] & A.Lakshmi Sudha[3]
[1]ASSOC.PROFESSOR. Department of EEE, PYDAH ENGG College, Kakinada, AndhraPradesh, INDIA
[2]PROFESSOR, JNTUH, Department of EEE, AndhraPradesh, INDIA.
[3]PG STUDENT,PRAGATI engg college,Kakinada,AP,INDIA

ABSTRACT

Outcome of DC-link capacitor voltage variation on inverter switching states is accessible and designed for three-level inverter. In this paper for back-to-back system by including five-level diode clamped topologies we are proposing a novel DC link balancing method. The algorithm which we proposed here is the improvement of variable switching frequency control policy which was previously introduced by means of three-level back-to-back system which depends on calculations of adjacent capacitor voltages which focuses on three-level DC link network to identify the information about potential variation in consecutive nodes. As per the above proposal, all four capacitors in DC link network are effectively balancing the voltage. Due to optimization of switching losses the proposed method has advantages over the variable switching frequency.

Keyword: *Multi level Inverter voltage balance Switching states Dc-link power factor.*

1. INTRODUCTION

Recent day's medium voltage and high power applications are using multilevel inverters which attracted much as compared to previous inverters. In this paper we used the most favorable among various multilevel configurations called neutral point clamped (NPC) inverter also known as Three-level diode-clamped inverter. Effects of neutral-point voltage unbalance and its various balance control methods are described elaborately [1]. Nuisance over voltage or under voltage trips are mainly caused due to increase in regenerative load which happens when there is overstress on capacitors by Unbalanced DC-Link. For which an active front-end along with coordinated control from grid-end and load-end to DC-Link balancing control [1]. We analyze transient and steady state condition for the effect of capacitor voltage unbalance. To reduce the output waveforms to two-level from normal three-level at worst case we unbalance one capacitor by fully charging to full DC-Link Voltage which results in switching devices and capacitors. We extensively analyzed many system parameters of three-level NPC inverter like value of capacitance of capacitor, modulation index, load power factor and load current by the effect of zero sequence voltage on the neutral point variation and the dependence of DC-link voltage. The redundant switching states are effectively used for neutral point balancing schemes to clamped inverters of the three-level neutral point. In place of neutral point voltage unbalance the redundant switching states are used alternately to the total unbalance in one switching cycle to zero [4-5]. Exhaustive analysis of space vectors, pulse pattern arrangement with division of middle regions for neutral point balance, NPC inverter, dwell timings and even harmonic elimination scheme were addressed [5]. By effective utilization of distribution of the redundant voltage vectors and phase current polarity we can achieve neutral point voltage control. By maintaining average current drawn from neutral-point to the minimum we propose a control strategy [6-7]. Hysteresis control for DC-link variation control and common mode voltage elimination in an open end winding induction motor fed from two three-level inverters from either side is investigated [8]. Proposal for Hysteresis control for DC-link variation control and common mode voltage elimination in an open end winding induction motor fed from two three-level inverters from either side is investigated from neutral-point control with charge balance and mathematical modeling [9]. ANN based neutral-point self-voltage balancing SVM with pulse pattern arrangement is discussed for NPC inverter. It requires extra switching when reference vector changes sector. [10]. In this paper we eliminated the problem of requirement of extra switching at sector changeover and validated experimentally on mathematical modeling and simulation results [11]. The SVM which we proposed in the paper uses redundant switching states which have opposite effects on DC-Link capacitor voltage for the inventor voltage vector which indeed have unbalancing effect on the capacitor voltages. So the utilization of redundant switching states overcomes the need for additional hardware for the capacitor voltage balancing by not affecting the dwell timing space vector over switching period.

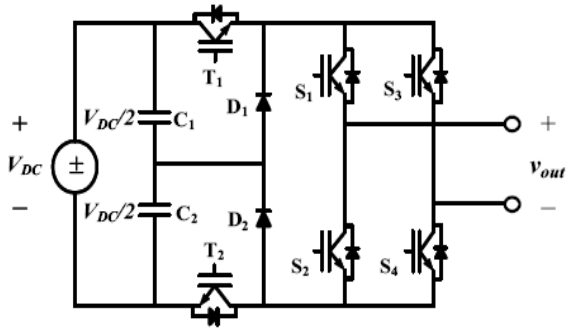

Fig.1: Multi level inverter

By considering neutral point voltage for various modulation index (MI) and DC-link voltages, inverter output voltage, Current THD the performance of various SVM methods are executed. By considering multi-level diode clamped topology the problem of capacitor imbalance can be resolved in two ways ; first way by four full-wave bridge rectifier and by providing particular voltage level from an isolated winding transformer with input AC-side interconnected primary[1]; second way with a back-end multi-level DC-AC converter to back-to-back connection of a front-end AC-DC multi-level converter. Where the first way is very not possible as size-wise and cost-wise and the second way is very much suitable because [3] with the back-end active-rectifier interfaced to a constant frequency/voltage input of the utility [4] or variable frequency/voltage input of the generator [5]. In all the three phases the front-end produces a voltage source inverter which is symmetrically and asymmetrically operable where as the back-end improves the active-rectifier with power factor correction on an input Ac-Side which reaches the utility criteria of harmonic alteration.

2. MULTILEVEL INVERTER TOPOLOGIES

Different types of Multilevel Inverters are as follows:

a) Diode-clamped multilevel inverter.
b) Flying-capacitor (capacitor-clamped) multi level inverter.
c) Cascaded-inverter with separate DC voltage sources.

II (a). Capacitor-Clamped Multilevel Inverter (Flying -Capacitor Multilevel Inverter)

The topology was first proposed by Meynard and Foch [14, 15, and 16]. The basic structural block diagram of a phase-leg capacitor-clamped inverter as shown in Fig.2 where the circuit can also be called as flying capacitor inverter [1], [9], [10] which provides a five-level output across A and N which has set of independent capacitors clamping the device voltage to one capacitor voltage level.

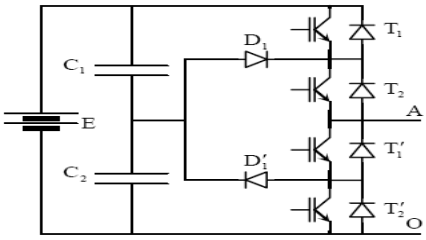

Fig.2: Three-level Capacitor-Clamped Multilevel inverter

As compared to diode-clamped converter the three-level capacitor clamped converter has more flexibility at voltage synthesis. Considering Fig.2 the voltage of the five-level phase-leg a output with respect to the neutral point n, V_{an}, can be synthesized by the following switch combination

1) For voltage $V_{an} = V_{dc}/2$, turn on all upper switches S_1-S_4.
2) For Voltage level $V_{an} = V_{dc}/4$, there are three combination,
3)

a) S_1, S_2, S_3, S_1' ($V_{an} = V_{dc}/2$ of upper C_4's – $V_{dc}/4$ of C_1);
b) S_2, S_3, S_4, S_4'(V_{an} =3 $V_{dc}/4$ of C_3's – $V_{dc}/2$ of lower C_4's);
c) S_1,S_3, S_4, S_3'($V_{an} = V_{dc}/2$ of upper C_4's -3 $V_{dc}/4$ of C_3's + $V_{dc}/2$ of C_2's)

4) For voltage V_{an} = 0, there are six combination

a) S_1, S_2, S_1', S_2' ($V_{an} = V_{dc}$ /2- V_{dc} /2)
b) S_3, S_4, S_3', S_4' ($V_{an} = V_{dc}$ /2- V_{dc} /2)
c) S_1, S_3, S_1', S_3' ($V_{an} = V_{dc}$ /2-3 V_{dc} /4+ V_{dc} /2-Vdc/4)
d) S_1, S_4, S_2', S_3' ($V_{an} = V_{dc}$ /2 – V_{dc} /3+ V_{dc} /4)
e) S_2, S_4, S_2', S_4' (V_{an} =3 V_{dc} /4- V_{dc} /2+ V_{dc} /4- V_{dc} /2)
f) S_2, S_3, S_1', S_4' (V_{an} =3 V_{dc} /4- V_{dc} /4- V_{dc} /4- V_{dc} /2)

5) For voltage V_{an} = - V_{dc} /4, there are three combination
a) S_1, S_1', S_2', S_3' ($V_{an} = V_{dc}$ /2- 3 V_{dc} /4)
b) S_4, S_2', S_3', S_4' ($V_{an} = V_{dc}$ /4- V_{dc} /2)
c) S_3, S_1', S_3', S_4' ($V_{an} = V_{dc}$ /2- V_{dc} /4 - V_{dc} 2)

6) For voltage V_{an} = - V_{dc} /2, Turn on all lower switches S_1'-S_4'

Table [1]: Operation Modes for Reference voltage and output voltage

Operating Mode	Reference voltage range	Output voltage
Mode 1	$Vc \leq V_{ref} < 2V_c$	$V_{dc}/2$ or V_{DC}
Mode 2	$0 \leq V_{ref} < V_c$	0 or V_{DC}
Mode 3	$-Vc \leq V_{ref} < 0$	$-V_{dc}/2$ or 0
Mode 4	$2Vc \leq V_{ref} < -V_c$	$-V_{dc}$ or $-V_{DC}/2$

Table [2]: Output voltage & Switching states

Output Voltage	Switching condition					
	S1	S2	S3	S4	T1	T2
V_{DC}	ON	OFF	OFF	ON	ON	ON
V_{DC}	ON	OFF	OFF	ON	OFF	ON
	ON	OFF	OFF	ON	ON	OFF
0	ON	OFF	OFF	ON	OFF	OFF
	OFF	ON	ON	OFF	OFF	OFF
$-V_{DC}/2$	OFF	ON	ON	OFF	OFF	ON
	OFF	ON	ON	OFF	ON	OFF
$-V_{DC}$	OFF	ON	ON	OFF	ON	OFF

3. THREE-LEVEL INVERTER

In Three-Level Neutral Point Clamped Inverter (NPCI) [12], the inverter leg 'a' has a collection of four IGBT type of switches named as S1,S2,S3 and S4 which are anti-parallel to four diodes named D1,D2,D3 and D4 where the DC bus capacitor is divided into two by providing a neutral point 'n' as in Fig.3. When S2 and S3 switches turned on the output terminal of the inverter is connected to neutral point using clamping Diodes Dn1 and Dn2 where the voltage through each DC capacitor is Vdc/2, which is nearly half to DC-Link Voltage Vdc. Using finite voltage values to C1 and C2 they can be charged or discharged by neutral current which causes deviation in neutral point voltage. Depending on operating condition of NPC inverter the neutral point voltage Vn varies. A premature failure of the switching devices may occur when neutral point voltage Vn varies too far which may cause to increase in harmonic for output voltage of inverter. As in Table [I] the operating status of switches in Neutral Point Clamped Inverter can be represented. Switching state 'P' denotes that the upper two switches in leg 'a' are on and the inverter pole voltage Va, which is ideally +Vdc/2, whereas 'N' indicates that the lower two switches conduct, leading to Va = -Vdc/2. Switching state 'O' signifies that the inner two switches S2 and S3 are on and Va is clamped to zero through the clamping diodes. Any of one among two clamming diodes are tuned ON depending on direction of Load Current ia. Terminal 'a' is connected to neutral point 'n' using the conduction of Dn1 and S2 to a positive load current(ia>0) forces Dn1 to ON. Similar to Switches like S2 and S4 the S1 and S3 are operated in complementary order. Using three switching states N,O and P the inverter phase can be represented. By considering all the three phases into account a combination of 27 switching states are there for inverters which is corresponding to 19 voltage vectors for

Three-Level Neutral Point Clamped Inverter and placement of vector in sector as in Fig.4. Voltage Vector can be categorized to four depending on magnitude as Large vector(uL), Medium Vector(uM), Small Vecotr(uS) and Zero Vector(uO) where they vary depending on magnitudes like zero magnitude for Zero Vector, magnitude of Vdc/3 for Small Vector where it has two switching states like P and N which can be classified as P-Type and N-Type Vectors , magnitude of Vdc/3 Medium Vector and magnitude of 2Vdc/3 for Large Vector.

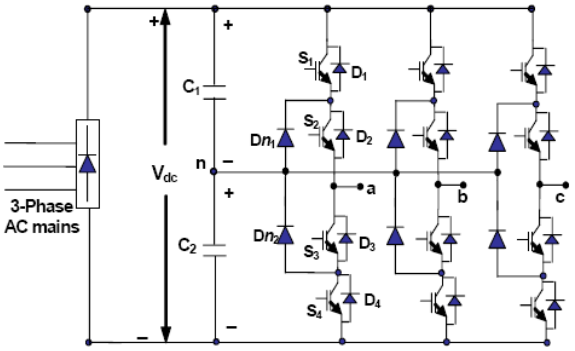

Fig.3: Three-level neutral-point clamped inverter topology

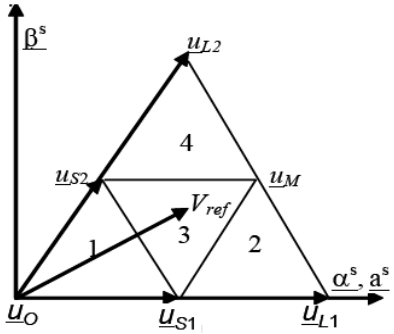

Fig.4: Space-vector diagram showing switching states (top) and Vector placement for SVPWM in sector A (bottom)

4. DC-LINK CAPACITOR VOLTAGE BALANCING SCHEME

By using open loop or closed loop schema many Space Vector Modulation Schemes (SVM) are proposed to Three-Level Neutral Point Clamped Inverter [11]. Over a sampling period of time the dwell time for a given small vector is equally distributed in between N and P-Type switching states to reduce neutral point voltage deviation. Either one or two small vectors among selected vectors are present for Nearest Three Vector (NTV) selection according to the triangular regions in which the reference vector Vreflies. If Vref is in 2 or 4 region then NTV has only one small vector if it is in 1 or 3 the NTV has two small vectors which is displayed in Fig.2.

*A. 7-Segment SVM or SVM-*1

Seven-segment pulse pattern will pulse pattern arrangement for region A1 when it is chosen for all four regions in SVM-1 as shown in Fig.4. Where it divides dwell time of only one small vector in P-type and N-type out of two small sectors available in region 1 and 3. That is the reason where neutral point deviation is not minimized in SVM-1.

B. SVM-2

By optimizing the pulse patter arrangement we can reduce neutral-point voltage variation according to the location of region. As in the Fig.5 we use two small vectors to neutral point voltage control for regions 1 and 3we use positive and negative sequences of modified SVM pulse pattern arrangement for regions A1, A2, A3, and A4 of sector A for one sampling period and we use 6 negative sequence (NEG_SEQ) pulse patterns are arranged in exact reverse order of positive sequence (POS_SEQ) pulse pattern and vice versa where they are switched alternatively. In sampling period Ts for modified SVM the numbers of switching per phase have two in region 1, one or two in region 3 and one in both 2 and 4. Where as in conventional SVM for sampling period Ts it requires two switching per phase here Ts is the combination of sequence of dwell times of NTV. Close loop modified SVM with 7, 9 & 13-segment pulse pattern arrangements and delta correction in dwell time is implemented for improved neutral point

voltage stabilization. There are chances where existence of small-voltage in every switching sequence whose dwell times are divided to sub periods like P-Type and N-Type switching states. Considering a scenario where the dwell time ds1p for **uS1p** and dS1n for **uS1n**, which is half/half split normally, can be distributed as

ds1 = dS1p + dS1n
where dS1p and dS1n are given by
dS1p = ds1 /2(1+Δt) and
dS1n = ds1 /2(1-Δt) where -1<= Δt<=1 … (1).

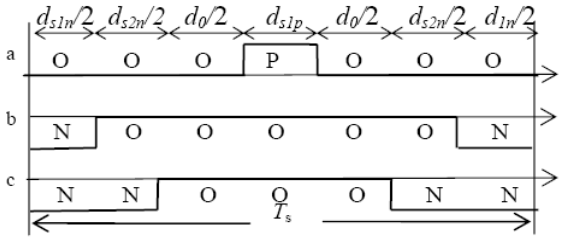

Fig.5. Pulse pattern arrangement for conventional seven-segment SVPWM in region A1

By considering the DC capacitor voltage Vci and Vc2 the variation of NPV can be reduced simply adjusting the incremental time Δt in (1). The difference in the capacitor voltage ΔvC where, ΔvC = vC2 - vC1 is the input to the voltage balancing scheme. If ΔvC is greater than the maximum allowed DC voltage deviation ΔVm for some reasons, we can increase dwell time dS1p and decrease dS1n by Δt (Δt>0) simultaneously for the inverter in a inverting mode. When the inverter is in converting mode a reverse action (Δt<0) has to be considered. Association of capacitors voltage difference and the incremental time interval Δt is summarized in table [2].

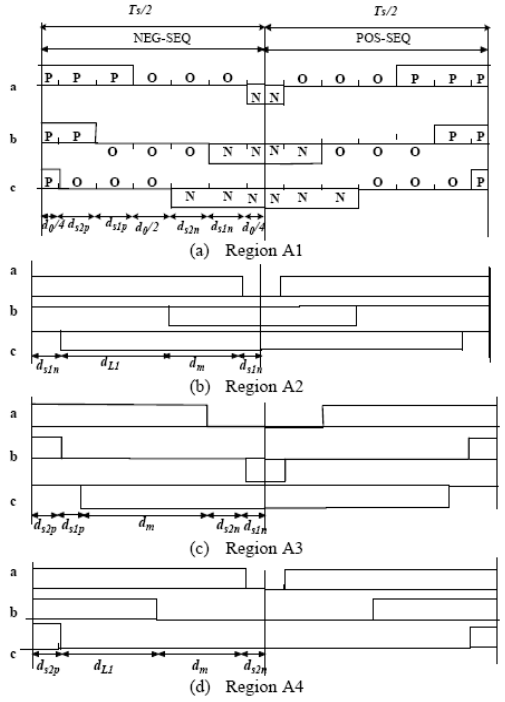

Fig.6: Pulse pattern arrangement of SVM-2 in sector A

5. RESULTS AND DISCUSSIONS

By considering laboratory prototype of diode clamped 3-level inverter the experimental results were calculated where a DC-Link Voltage of 100 volts and DC-Link capacitance of 2200uF and for Inductive Load a Resistance of 10ohm and inductance value of 160mH are used as. And output waveform quality of Three-Level Inverter at MI value of 0.8 is generated as shown in Fig.8. Harmonic spectrum revels that higher even order harmonic components increases voltage and current THD due to large unbalance in DC-link voltages. The phase voltage THD versus MI for SVM-1 and SVM-2 are plotted in Fig.9. Where the dwell time of small vector can be reduced at MI value of

0.866. By splitting small vector the DC-Link voltage balancing becomes inefficient. The proposed scheme is more efficient and effective to control in regions of 1 and 3 where in which two small vectors are spitted in pulse pattern arrangement for DC-Link balancing control. Where as in region 2 and 4 only one small vector is spitted in pulse pattern arrangement for DC-Link balancing control. In the proposed the NPV is controlled below maximum specified value as compared to DC-Link voltage for SVM-1. And in proposed scheme the NPV of SVM-2 is comparably low to NPV of SVM-1.

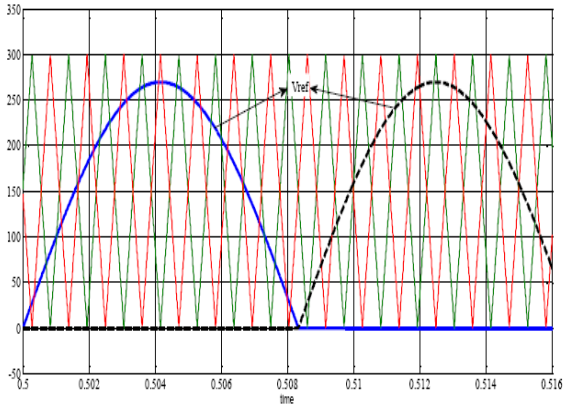

Fig.7: Sine triangle PWM for split natural balancing

Power Factor Effects: Considering operations at unity power factor or values close to it many research has been done on FCML converters. A load current characteristic has more effected by power factor even though it does not effect capacitor voltage. The power factor 0.9 and 0.3 are identified as capacitor voltages Vca and Vcb as shown in Fig.8 where we can observe capacitor voltage characteristics shows not that much difference with the difference in power factor.

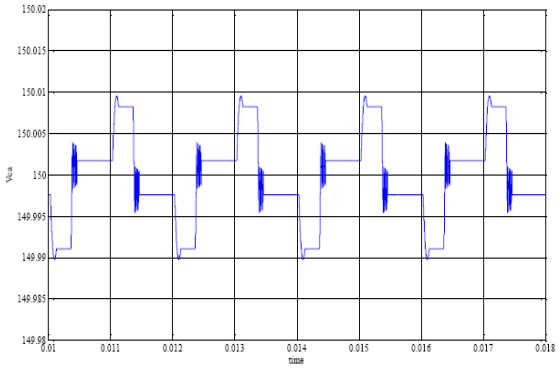

Fig8: Output waveform quality of the 3-level inverter (Capacitor voltage *Vca* at PF=0.9)

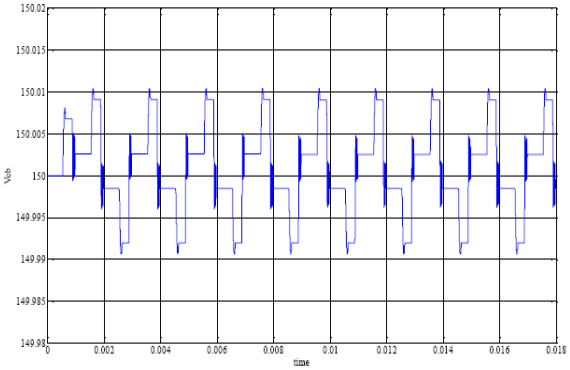

Fig9: shows plot of phase voltage THD versus MI for SVM-1 and SVM-2(Capacitor voltage *Vcb* at PF=0.9)

6. CONCLUSION

By considering Three-Level Diode Clamping we investigated the DC-Link voltage balancing scheme, and analyzed the behavior of DC-Link Voltage control behavior on SVM-1, SVM-2 schemas and on proposed scheme. Using

simple control technique like Redundant space vectors, their sequencing, and splitting of their duty cycle we proposed the closed loop scheme. To reduce the cost and volume we used single front end rectifier with reduced rating DC-Link capacitor. By considering several DC-Link Voltages and Modulation Index (MI) we evaluated various schemes with respect to NPV reduction, Inverter output voltage THD and Current THD. The scheme which is proposed in this paper reduces the Neutral Point Voltage considering major harmonic loss minimization and effective voltage balancing control which gives long lasting life for DC-Link capacitor.

REFERENCES

[1]. F. Wang, "Multilevel PWM VSIs: Coordinated control of regenerative three-level neutral point clamped pulse widthmodulated voltage source inverters", *IEEE Industrial Applications Magazine*, July-August 2004, pp. 51-58.

[2]. S. Ogasawara, and H Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM Inverters", *Proceedings IEEE Industrial Applications Society Conference*, 1993, pp. 965-970.

[3]. K. R. M. N. Ratnayake, Y. Murai and T. Watanabe, "Novel PWM scheme to control neutral point voltage variation in three-level voltage source inverter", *Proceedings of IEEE Industrial Applications, 34th IAS Annual Meeting Conference.*, vol. 3, pp.1950 – 1955, 1999.

[4]. R. Rojas, T. Ohnishi and T. Suzuki, "An improved voltage vector control method for neutral point clamped inverters", *IEEE Transactions on Power Electronics*, vol. 10, No. 6, pp. 666- 672, November 1995.

[5]. B. Wu, "High-Power Converters and AC Drives", *IEEE* Press and Wiley, pp. 143-176, 2006.

[6]. C. Newton, and M. Summer, "Neutral point control for multi-level inverters: Theory, design and operation limitations," *Proceedings of IEEE IAS Conference Reccordings*, 1997, pp. 1336-1343.

[7]. K. Yamanaka, A. M. Hava, H. Kirino, Y. Tanaka, N. Koga, and T. J. Kume, "A novel neutral potential stabilization technique using the information of output current polarities and voltage vector," *IEEE Transactions. On Industrial. Applications*, vol. 38, No. 6, pp. 1572-1580, November/December 2002.

[8]. Kanchan, R. S., Tekwani, P. N. and Gopakumar K., "Three-Level Inverter Scheme With Common Mode Voltage Elimination and DC-link Capacitor Voltage Balancing for an Open-End Winding Induction Motor Drive", *IEEE Transactions on Power Electronics*, vol. 21, No. 6, pp.1676-1683, November 2006.

[9]. G. Sinha and. T. A. Lipo, "A four-level inverter based drive with a passive front end", *IEEE Transactions Power Electronics*, vol. 15, No. 2, pp. 285-294, March 2000.

[10]. J. O. P. Pinto, B. K. Bose, L. E. B. Da Silva and M. P. Kazmierkowski, "Neural-network-based space-vector PWM controller for voltage-fed inverter induction motor drive", *IEEE Transactions on Industrial Applications*, vol. 36, No. 6, pp. 1628-1636, November/December 2000.

[11]. Pramod Agarwal and Kalpesh Bhalodi, "Space Vector Modulation with DC-Link Voltage Balancing Control for Three Level Inverters", conference proceedings on *IEEEPEDES- 06*, Dec-2006, New Delhi.

[12]. Kalpesh H. Bhalodi, and Pramod Agarwal "Space Vector Modulation with DC-Link Voltage Balancing Control for Three-Level Inverters" ACEEE International Journal on Communication, Vol 1, No. 1, Jan 2010