ELECTRICAL CHARACTERISTICS OF STRAINED DOUBLE GATE MOSFET

Hossein Valinajad [1] Reza Hosseini[2] & Mohhamad Esmael Akbari[3]
[1,3] Department of Electrical Engineering, Ahar Branch, Islamic Azad University,Ahar, Iran.
[2] Department of Electrical Engineering, Khoy Branch, Islamic Azad University, Khoy, Iran.
m-Akbari@iau-Ahar.ac.ir

ABSTRACT

In this paper electrical characteristics of Strained Double Gate Metal Oxide Semiconductor Field Effect Transistor(DG MOSFET) and that of Conventional Double Gate MOSFET were investigated. A quantum mechanical transport approach based on non-equilibirium Green's function(NEGF) method in the frame work of effective mass theory is employed in this analysis. We evaluate the variation of the threshold voltage, the subthreshold slope, ON state current when channel length decreases. It is shown that the strained DG MOSFET gives high performance transistor value of the scaled transcoductance and ON current that are greater than conventional DG MOSFET. Furthermore, comparison of unity current gain frequency f_T of the devices ,which represents key metric for device applications, shows that the performance of strained DG MOSFET is better than the conventional DG MOSFET.

Keywords: *Strain, DG MOSFET, NEGF, unity current gain frequency.*

1. INTRODUCTION

As the MOSFET gate length enters the nanometer regime, short channel effects ,such as Drain-Induced-Barrier-Lowering (DIBL), become more and more significant, thus, various device concepts such as DG MOSFETs is becoming extensively attractive [1-2]. A major impetus for using these devices is the improved gate control and the reduction in short channel behavior for them. Conventional CMOS technology is facing greater challenges in terms of scaling due to reduced gate control, increased short-channel effects (SCEs) and high leakage currents [3].
Double gate structures on undoped SOI (Silicon on Insulator) are promising to overcome short channel effects (SCE) in nanometer-scaled MOSFET. In addition, these devices exhibit a good I_{on}/I_{off} and present a channel with high conductivity[1]. DG MOSFETs have emerged as promising devices for nano-scale circuits due to their better scalability below 20 nm. Due to the presence of double gate, the effective gate control increases, reducing SCEs[4].
Improvement in the VLSI/ULSI circuit speed may be achieved by enhancement of the charging current of the device. This will be possible if new materials with higher carrier mobility are considered as replacement for conventional silicon or if novel methods are employed to enhance the carrier mobility such as applying strain in Si channel [5-7]. The use of strained Si/SiGe material promises the improvement of speed performance of CMOS devices.
In this paper we analyze Strained and conventional DG-MOSFET using a quantum mechanical transport approach based on non-equilibirium Green's function method in the frame work of effective mass theory [8-9], with assuming that channel length varies from 7nm to 20nm regime .

2. DEVICE STRUCTURES

2.1 Strained DG MOSFET

The strained DG MOSFET studied here is presented in Fig. 1. The channel of device is undoped, source and drain are highly doped($N_D= 10^{20}$ cm^{-3}) and those are in the same length ($L_{S,D}$=6.5nm). Aluminum has been used as metal gate with lateral SiO2 spacers partially covering source and drain regions. In this study, body length (T_{body}) is assumed 4nm, the thickness of SiGe layer is 1 nm, channel length (L_{ch}) varies from 7 nm to 20nm and the oxide thickness(t_{ox}) is 1nm.

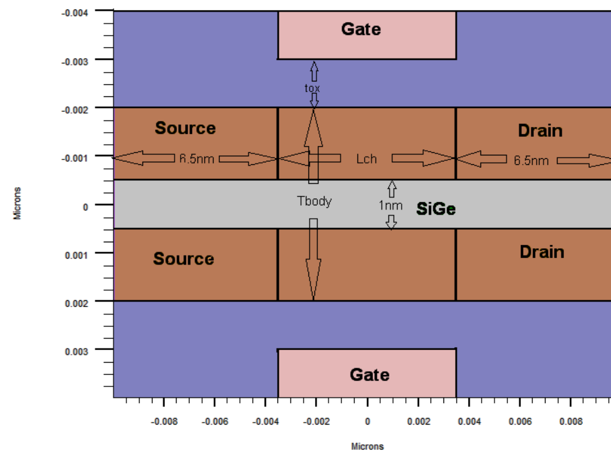

Figure 1. Strained DG MOSFET simulated in this paper. The channel of device is undoped ,source and drain are highly doped(N_D= 10^{20} cm^{-3}). Aluminum has been used as metal gate with lateral SiO2 spacers partially covering source and drain regions. T_{body} is 4nm, the thickness of SiGe layer is 1 nm, L_{ch} varies from 7 nm to 20 nm and t_{ox} is 1nm.

2.2 Conventional DG MOSFET

The Conventional DG MOSFET studied in this work is shown in Fig. 2. The channel of device is intrinsic silicon ,source and drain are highly doped(N_D= 10^{20} cm^{-3}) and those are in the same length ($L_{S,D}$=6.5nm). Aluminum has been used as metal gate with lateral SiO2 spacers partially covering source and drain regions. In this study, body length (T_{body}) is assumed 4nm, channel length (L_{ch}) varies from 7 nm to 20 nm and the oxide thickness(t_{ox}) is 1nm.

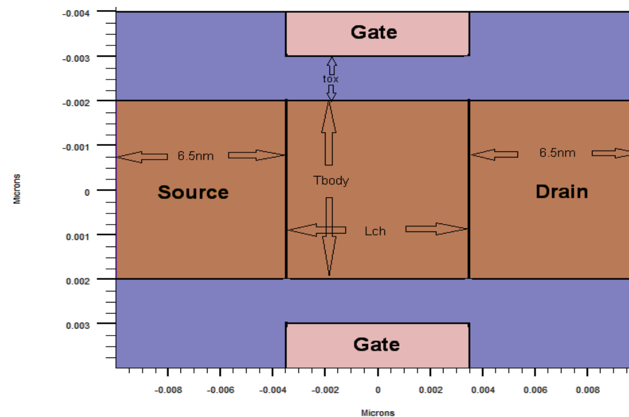

Figure 2. Conventional DG MOSFET simulated in this paper. The channel of device is intrinsic silicon ,source and drain are highly doped(N_D= 10^{20} cm^{-3}). Aluminum has been used as metal gate with lateral SiO2 spacers partially covering source and drain regions. T_{body} is 4nm, L_{ch} varies from 7 nm to 20 nm and t_{ox} is 1nm.

3. SIMULATION METHOD

In the nanometer regime, the wave-like behavior of Electron becomes significant, and the tunneling current should be considered. So the semiclassical transport equation is not suitable. In this paper we use a quantum mechanical approach based on non-equilibrium Green's function and employ uncoupled mode space (UMS) approach[9-10].
Here. the quantum confinement is in one dimension (along Y axis), the calculation of the quantum electron density relies upon a solution of a 1D Schrodinger equation solved for eigen state energies $E_{iv}(x)$ and wavefunctions $\Psi_{iv}(x,y)$ at each slice perpendicular to the X axis and for each electron valley ν[11]

$$-\frac{\hbar^2}{2}\frac{\partial}{\partial y}\left(\frac{1}{m_y^v(x,y)}\frac{\partial \psi_{iv}}{\partial y}\right)+E_C(x,y)\psi_{iv}=E_{iv}\psi_{iv} \qquad (1)$$

Where m^v_y (x,y) is a spatially dependent effective mass in Y direction for the ν-th valley and $E_C(x,y)$ is a conduction band edge.The conduction band of silicon is characterized by anisotropic effective masses ml and mt, where ml and mt are the longitudinal and transverse effective masses, respectively.
In practice, due to strong quantum confinement, usually only a few of the lowest subbands are occupied and need to be included in the calculations. On the other hand, subbands are uncoupled and transport equation is a 1D equation. Transport is computed by NEGF formalism in 1D subbands within the mode space approach.
The self-consistent loop starts with an initial guess for the potential. Then, Schrodinger equation is solved using this potential and the electron density are computed as follows[11]:

$$n(x,y) = 2\frac{2k_BT}{\pi\hbar^2}\sum_v \sqrt{m_x^v(x,y)m_z^v(x,y)}\sum_{i=0}^{\infty}|\psi_{iv}(x,y)|^2 \ln\left[1+\exp\left(-\frac{E_{iv}-E_F}{k_BT}\right)\right] \quad (2)$$

Then, this density is fed back into the Poisson solver for the self-consistent calculation. Once convergence is achieved, the current is computed as shown below[9]:

$$I = \frac{q}{2\pi\hbar}\int_{-\infty}^{+\infty} T(E)[f_{1D}(\mu_S - E) - f_{1D}(\mu_D - E)]dE \quad (3)$$

$$T(E) = \sum_{m=1}^{M} T^m(E) \quad (4)$$

$$T^m(E) = Trace\left(\Gamma_S^m(E)G^m(E)\Gamma_D^m(E)G^{m\dagger}(E)\right) \quad (5)$$

$$\Gamma_S^m(E) = i(\sum_S^m(E) - \sum_S^{m\dagger}(E)) \quad (6.a)$$

$$\Gamma_D^m(E) = i(\sum_D^m(E) - \sum_D^{m\dagger}(E) \quad (6.b)$$

where T(E) is the transmission function and is obtained by summing the transmission function for each subband, q is the electron charge, h is Plank's constant, G^m is Green's function and $\sum^m_S$ and $\sum^m_D$ are self-energies for the source and the drain.[19]
Von Neumann boundary condition is used for potential in the source and drain. This type of boundary condition is required in ballistic devices to ensure the charge neutrality in the source and the drain region[9]. Also, Dirichlet boundary condition is applied to the gate contact[8].

4. RESULTS AND DISCUSSION

The tensile strained-Si layer causes the energy levels of four fold and two fold valleys to split and the energy levels of two fold valleys to be located lower than that of four folds[8]. The energy band model for relaxed SiGe and strained-Si is generated based on Ref. [12]. The material properties are summarized in table 1.
Figure 3 represents the source - drain current as a function of gate voltages for Strained DG MOSFET when V_{DS} is equal to 0.5V and channel length varies from 7nm to 20nm. Similar I-V characteristic for Conventional DG MOSFET has been shown in Figure 4. It can be seen that the reduction of the channel length results in shifting the characteristics to the left and it is clear that as the channel length become smaller than 15nm, the subthreshold current rises dramatically. Since the drain current depends on the channel length, the threshold voltage of the devices should also be channel length dependent.
Electrical characteristics for Strained and conventional DG MOSFET are summarized in table I and table 2. It shows that threshold voltage is proportional to L_{ch} for both devices.

Table 1. Material properties used in this work (x is the Ge content in the $Si_{1-x}Ge_x$)[12].

Parameter	Eq.used
Electron affinity	$\chi_{Strained-Si} = 4.05 + 0.58x$ $\chi_{SiGe} = 4.05 - 0.05x$
Band gap energy	$E_{g,Strained-Si} = 1.12 - x(0.31 + 0.53x)$ $E_{g,SiGe} = 1.12 - 0.42x$
Conduction band offset	$\Delta E_C = 0.63x$
Valance band offset	$\Delta E_V = x(0.74 - 0.53x)$

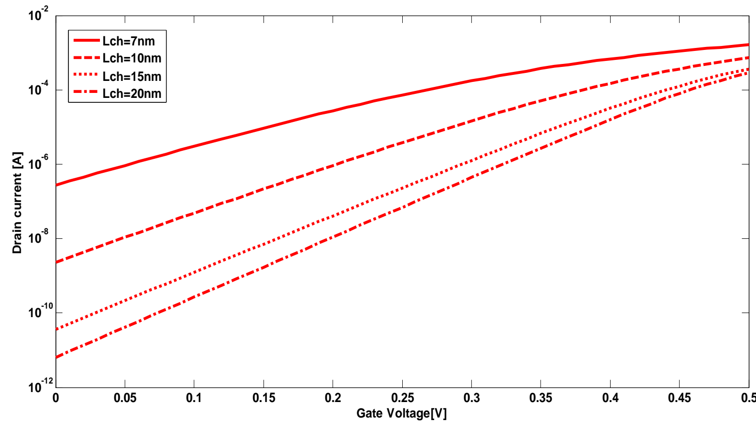

Figure 3. Drain current versus gate voltage for strained DG MOSFET when channel length varies from 7nm to 20 nm at V_{DS}=0.4V.

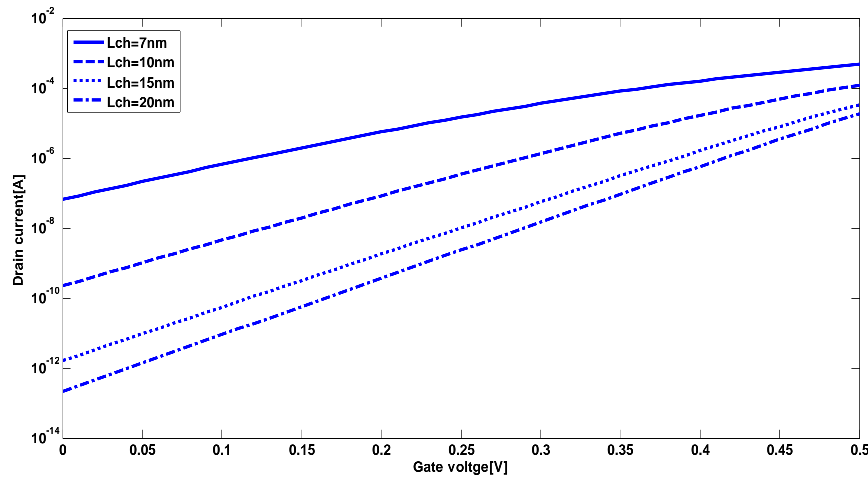

Figure 4. Drain current versus gate voltage for conventional DG MOSFET when channel length varies from 7nm to 20 nm at V_{DS}=0.4V.

In table 2, ON current is given for strained DG MOSFET and in table 3 it has been given for conventional DG MOSFET. ON current is computed current when V_{DS}=0.4V and V_{GS}-V_{TH}=0.3V [13]. It is observed I_{ON} in the Strained structure is more than the other. Also, it can be seen the subthreshold slope and DIBL in the Strained structure is relatively smaller than those in the conventional structure.

Table 2. Simulation Results for strained DG MOSFET.

	L_{ch}=7nm	L_{ch}=10nm	L_{ch}=15nm	L_{ch}=20nm
Threshold Voltage(V)	0.195	0.248	0.281	0.292
Subthreshol Slope(mV/dec)	93.4	74.9	65	62
DIBL	0.522	0.487	0.483	0.441
ON Current (A/μm)	1.57×10^{-3}	1.15×10^{-3}	1.06×10^{-3}	9.63×10^{-4}

Table 3. Simulation Results for conventional DG MOSFET.

	L_{ch}=7nm	L_{ch}=10nm	L_{ch}=15nm	L_{ch}=20nm
Threshold Voltage(V)	0.242	0.302	0.328	0.341
Subthreshol Slope(mV/dec)	97.7	76	66	64
DIBL	0.579	0.521	0.501	0.496
ON Current (A/µm)	6.75×10^{-4}	4.55×10^{-4}	3.44×10^{-4}	3.2×10^{-4}

Figure 5 shows the variations of drain current with drain voltage at $V_{GS}-V_{TH}$ = 0.3V for L_{ch} = 7 nm. The drain current in the strained DG MOSFET is larger than the drain current for other structure.
Figure 6 shows simulated transconductance characteristics at the drain bias of 0.4 V of strained and conventional DG MOSFET with the channel length of 7 nm. It indicates that the transconductance of strained structure is enhanced at high gate drive, compared with that of conventional structure. This enhancement in transconductance of strained DG MOSFET is due to the electron velocity improvement.

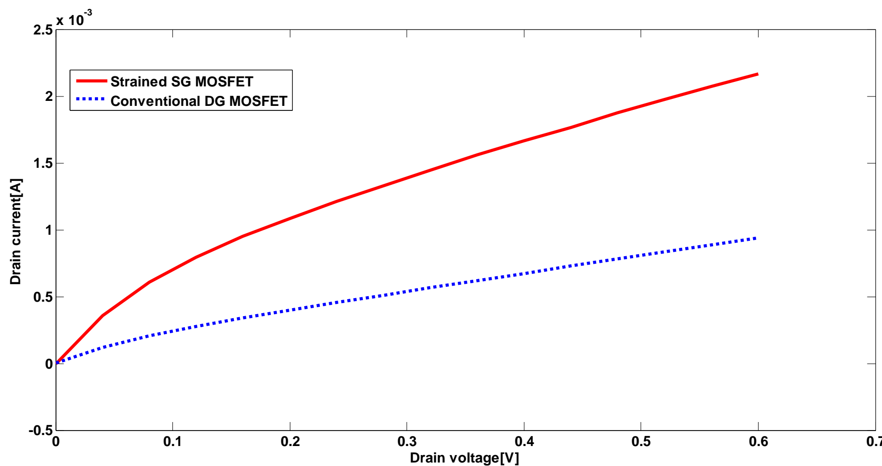

Figure 5. Drain current versus drain voltage strained and conventional DG MOSFET at L_{ch} = 7 nm, when $V_{GS} - V_{TH}$ = 0.3 V.

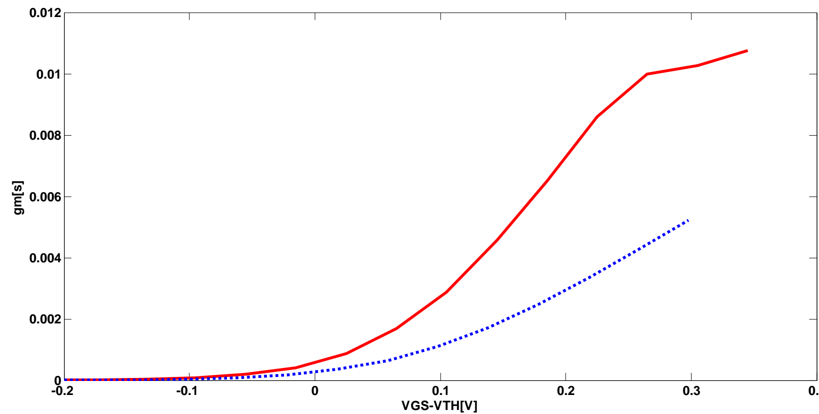

Figure 6. Transconductance for strain and conventional DG MOSFET versus $V_{GS} - V_{TH}$ when L_{ch} = 7nm and V_{DS} = 0.4V.

The gate-source capacitance is series combination of the oxide and quantum capacitance as below[15]:

$$C_{GS} = [C_{OX}^{-1} + C_{Q}^{-1}]^{-1} \qquad (7)$$

C_{OX} is classical capacitance and can be analytically obtained as[16]

$$C_{OX} = \frac{2\pi\varepsilon_0\varepsilon_r}{Ln\left[\frac{(2T_{OX}+T_{body})}{T_{body}}\right]} = 550\,pF.m^{-1} \quad (8)$$

where ε_r is the oxide dielectric constant, ε_0 is the permittivity of vacuum, t_{OX} is the oxide thickness and Tbody is diameter of body. Quantum capacitance can be defined as[16]

$$C_Q = q^2 \frac{\partial n}{\partial E_{FS}} \quad (9)$$

Figure 7 shows the variation of the gate capacitance for strained and conventional DG MOSFETs as a function of $V_{GS}-V_{TH}$ when L_{ch} = 7 nm. A lower capacitance is obtained for the strained structure. In Figure 7, we can see the intrinsic unity current gain frequency which is calculated from $f_T = g_m/2\pi C_g$.The unity current gain frequency f_T in strained DG MOSFET is higher than that in conventional structure because of high transconductance and low capacitance in strained device(figure 8).

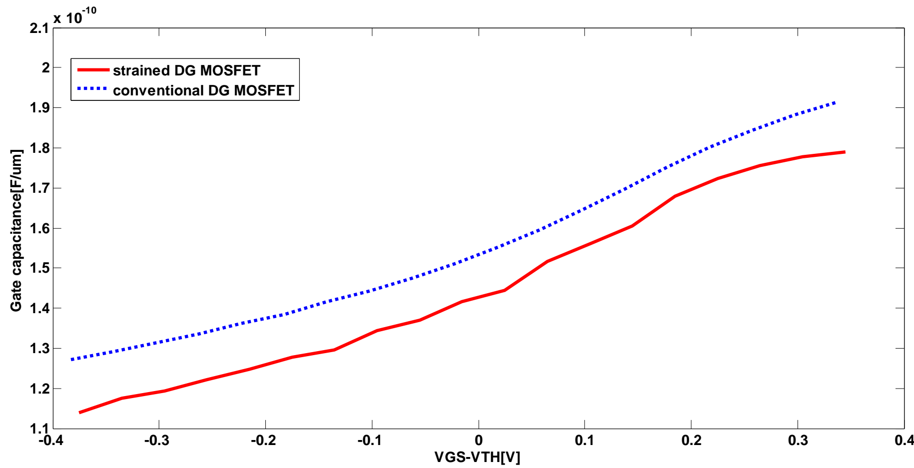

Figure 7. Gate capacitance for strained and conventional DG MOSFET versus $V_{GS} - V_{TH}$ when L_{ch} = 7 nm and V_{DS} = 0.4V.

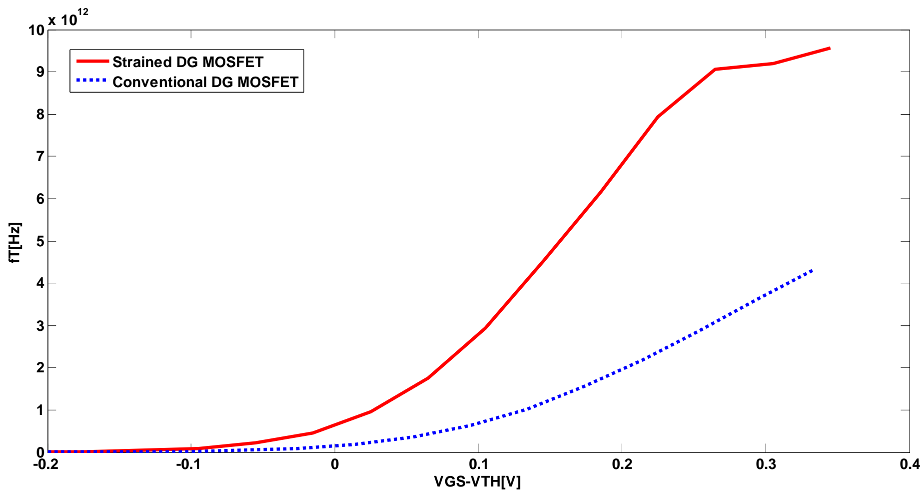

Figure 8. Intrinsic unity current gain frequency (f_T) for strained and conventional DG MOSFET when L_{ch} = 7 nm and V_{DS} = 0.4 V.

5. CONCLUSION

In this paper, we have analyzed a strained channel DG MOSFET for higher speed CMOS circuits. We employed quantum mechanical transport approach based on non-equilibrium Green's function method in the effective mass

approximation. Von Neumann boundary condition was used in the source/drain and Dirichlet boundary condition for the gate contact. The electrical characteristics for this structure have been investigated in detail for different channel length. It was revealed that the drain current for the strained channel DG MOSFET was improved when compared to the conventional DG MOSFET. Strained DG MOSFET presents lower DIBL effect , lower sub-threshold slope and higher ON current.

The gate capacitance and transconductance of the strained DG MOSFET increased which resulted in improved unity current gain frequency in comparison with conventional DG MOSFET. Consequently, strained device is expected to be a promising transistor for high-frequency applications in ultra small scales.

6. REFERENCE

[1] X. Loussier, D. Munteanu, J.L. Autran, ‘Simulation study of circuit performances of independent double-gate (IDG) MOSFETs with high- permittivity gate dielectrics ’,2009, J. Non-Cryst. Solids,vol.355,pp.1185-1188

[2] D Rechem, S Latreche and C Gontrand 'Channel length scaling and the impact of metal gate work function on the performance of double gate-metal oxide semiconductor field effect transistors' journal of physics ,Indian Academy of Sciences, Vol. 72, No. 3, pp. 587-599

[3] Saibal Mukhopadhyay,Keunwoo Kim, Ching Te Chuang and Kaushik Roy, Modeling and Analysis of Leakage Currents in Double-Gate Technologies, IEEE Transactions on Computer -Aided Design of Integrated Circuits and System, Vol. 25, NO. 10,2006

[4] Te-Kuang Chiang, A new two-dimensional subthreshold behavior model for the short-channel asymmetrical dual-material double-gate (ADMDG) MOSFET’s' Microelectronics Reliability 49 (2009) 693–698

[5] Tomohisa Mizuno, Naoharu Sugiyama, Tsutomu Tezuka, Yoshihiko Moriyama, Shu Nakaharai, Tatsuro Maeda, and Shin-ichi Takagi," High-Speed Source-Heterojunction-MOS-Transistor (SHOT) Utilizing High-Velocity Electron Injection" IEEE Transactions on Electron Device, Vol. 52, No. 12, 2005

[6] Kidong Kim, Ohseob Kwon, Jihyun Seo and Taeyoung Won" Two-Dimensional Quantum Mechanical Modeling for Strained Silicon Channel of Double-Gate MOSFET" Journal of the Korean Physical Society, Vol. 45, December 2004, pp. S909-S913

[7] Karol Kalna, Antonio Martinez, A. Svizhenko, M.P. Anantram, J.R. Barker, A. Asenov" NEGF simulations of the effect of strain on scaled double gate nanoMOSFETs" J Comput Electron (2008) 7: 288–292

[8] Hideyuki Iwata, Toshihiro Matsuda, and Takashi Ohzone" Influence of Image and Exchange-Correlation Effects on Electron Transport in Nanoscale DG MOSFETs" IEEE Transaction on Elctron Devices, Vol. 52, No. 7, 2005

[9] O Kurniawan, P Bai and E Li" Ballistic calculation of nonequilibrium Green’s function in nanoscale devices using finite element method" J. Phys. D: Appl. Phys. 42 (2009) 105109

[10] Mathieu Luisier, Andreas Schenk, and Wolfgang Fichtner" Quantum transport in two- and three dimensional nanoscale transistors: Coupled mode effects in the nonequilibrium Green’s function formalism" Journal of Applied Physics 100, 043713 ,2006

[11] Silvaco Int.: ATLAS Users Manual (2011), Device simulation Software, Silvaco International, Santa Clara, CA.

[12] Sh.T Chang, Nanoscale Strained Si/SiGe Heterojunction Trigate Field Effect Transistors, Jpn. J. Appl. Phys. 44 (2005) 5304

[13] K. Alam and M. Abdullah, Effects of dielectric constant on the performance of a gate all around InAs nanowire transistor, IEEE Trans. Nanotechnol. 11 (2012) 82.

[14] A.Seyedi, A.A.Pavel, A.K.Sharma, N.E.Islam,: ‘Design and performance analysis of a nanoscaled inverter based on wraped-around-gate nanowire MOSFETs’ 2009,Micro & Nano letters,Vol.4 , pp.16-21

[15] K. Alam and M. Abdullah, Effects of dielectric constant on the performance of a gate all around InAs nanowire transistor IEEE Trans. Nanotechnol. 11 (2012) 82.

[16] M. Khayar and R. Lake, The Quantum and Classical Capacitance Limits of InSb and InAs Nanowire FETs, IEEE Trans. Electron Devices 56 (2009) 2215.